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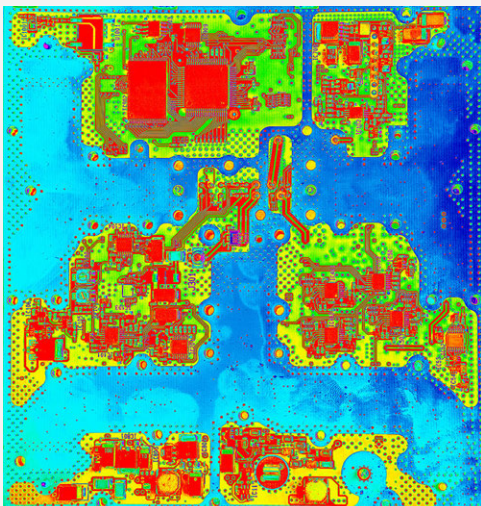
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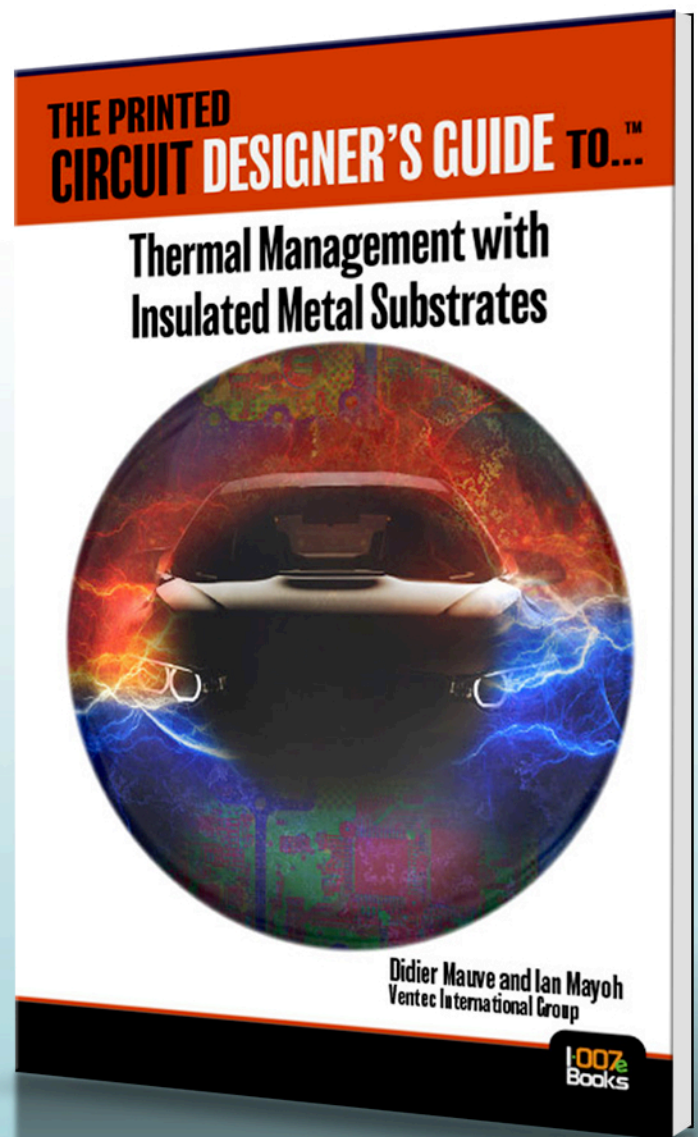
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Written by Didier Mauve and Ian Mayoh of Ventec International Group, this book highlights the need to dissipate heat from electronic devices.



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Tools & Technology

Today's EDA tools contain more horsepower than anyone could have imagined not long ago. For this issue of *Design007 Magazine*, we asked our expert contributors to discuss their newest software tools and technology, and the advantages of having the best tool for the job.



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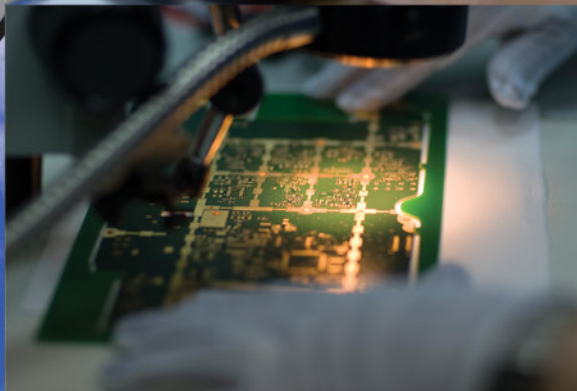
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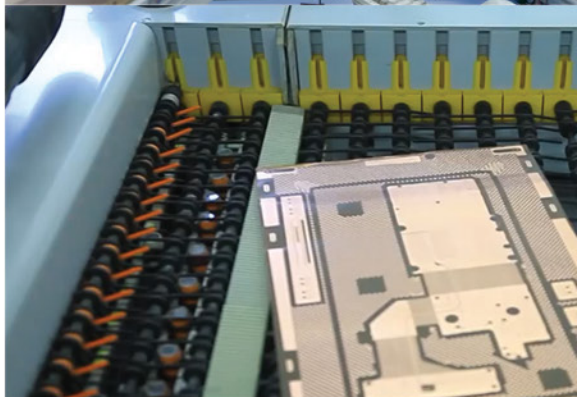
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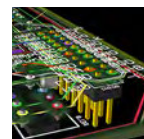


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IPC APEX EXPO, Tools and Technology

The Shaughnessy Report
by Andy Shaughnessy, I-CONNECT007

Another IPC APEX EXPO is history, and while it was a good show, I'm happy to be home. I'm sure my co-workers feel the same way, especially those who had to travel halfway around the world to attend.

This was another upbeat show; everyone was optimistic about the industry, and almost everyone was hiring. One company only recently stopped hiring after filling a slew of open positions. That's one of the downsides to nearly full employment: Potential employees can afford to be choosy, so jobs go unfilled for months, and existing employees don yet another hat in the meantime.

If I had to pick a theme for this year's IPC APEX EXPO, I would have to say that it was data. It seems that everyone from the PCB designer to the SMT process engineer has the tools they need to do their jobs just fine, but they're deluged with data. The real star of this show was the technology that helps PCB designers, fabricators and assemblers organize, manage, and access tons of data and present it as actionable information.

The week started with the Design Forum, which drew a pretty decent crowd. Here again, most of the presentations focused on managing design data, not actual PCB design



Photo credit: IPC

tips and techniques. Multek's Dana Korf and ThingWeaver's Gary Carter discussed efforts to develop a truly digital fab data package in one .XML file. As Dana said, over 90% of new designs arrive with incorrect and/or missing data, often in drawings and other hard copies. He explained why data must be completely digital for Industry 4.0 manufacturers to succeed. (He also pointed out that there are over 2,000 fab shops near his China office.)

Jan Pederson of PCB broker Elmatica discussed CircuitData, their new open source language that works with IPC-2581, Gerber and ODB++ , helping to organize the data handoff into a single file that fabricators welcome. Jan was careful to explain that he's here to work with, not replace, the existing data formats, and he encouraged any interested parties to get involved with this open language.

L3's Robb McCord, CID, covered some of the challenges designers face when exchanging files between ECAD and MCAD environments. He demonstrated a method that mapped MCAD IDF files to a new type of IDF file that can be imported by ECAD users, while an ECAD file can be exported as DFX and post-processed for use by MCAD engineers. Craig Armenti of Mentor also focused on ECAD-MCAD collaboration by way of IDX, and pointed out ways to address many challenges caused by this convergence of the different worlds.

TTM's Julie Ellis had a great presentation on design considerations that can increase cost and reduce manufacturability. As she said, if you don't need to have 3/3 spaces and traces, why not get 4/4 or 5/5? Some designers just make their boards needlessly expensive, though she added that she has her regular customers "trained" to give her the best designs for the job.

Out on the show floor, much of the chatter focused on IPC's demo of the new CXF (Connected Factory Exchange) protocol, which allows managers to check real-time stats on each SMT machine from a smartphone. I pulled it up on my phone, and I watched the temperature profiles and numbers of parts placed changing constantly. A process engineer might be able to telecommute a few days a week with more tools like this!

One item worth noting: DesignCon 2019 and IPC APEX EXPO 2019 take place the same week next year, September 29-31. This is going to be a big problem for companies who attend or exhibit at both shows. Some fabricators have booths at both shows, and some engineers teach classes at both shows. It'll be interesting to see how this works out.

Tool Time

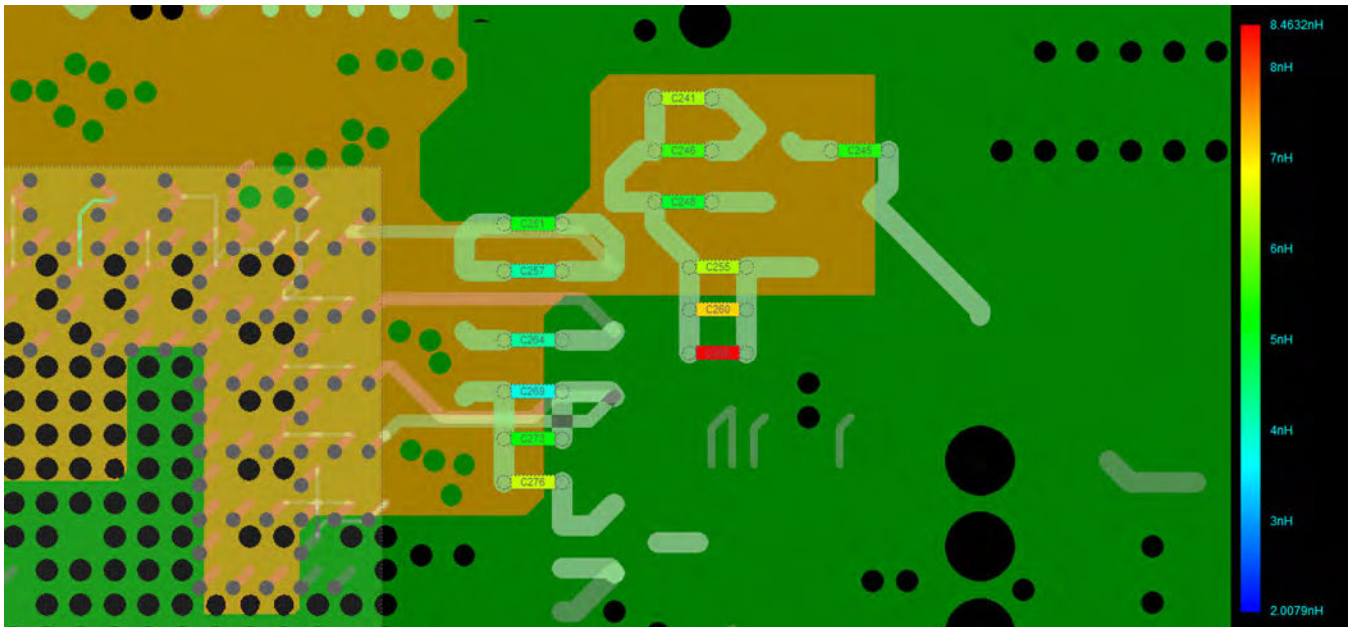
Design tool technology is better than ever, and PCB designers now work with EDA tools that contain more horsepower and functionality than anyone could have imagined not long ago. For this issue of Design007, our expert contributors discussed their newest tools and technology. First, Editor Kelly Dack sits down with Sam Chitwood of Cadence Design Systems to discuss the newest Sigrity power integrity software, and how it may help designers preclude so-called "exothermal events." Chuck Ferry of Mentor explains how HyperLynx now allows designers to automate SERDES channel validation early in the design process.

Columnist Tim Haag examines some of our newest technology and ponders whether this will help draw more young people into a PCB design career. Natasha Baker of SnapEDA explains how her small company creates so much of its technology from scratch, and how it has allowed the company to grow so much in only five years. And Arno Kolk of the Estonian Electronics Industries Association discusses the explosive growth of technology in his country in the past few decades.

It's hard to believe it's already March, but at least the snow has melted in Atlanta. See you next month! **DESIGN007**



Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 18 years. He can be reached by clicking [here](#).



Cadence's Sigrity Automates Power Integrity Simulation Earlier in Design Cycle

by Kelly Dack
GUEST EDITOR

DesignCon is always a great place to check out the latest PCB layout and simulation software tools. During DesignCon 2018, I met with Sam Chitwood, a product engineer with Cadence. Sam explained how the Cadence Sigrity simulation software now allows users to make decisions early in the design process, and how this can help optimize the design of the power delivery network and ensure signal integrity in complex PCBs.

Kelly Dack: I'm here at DesignCon with Sam Chitwood. I understand that the Sigrity tools now address some power integrity methodology issues. Why don't we start talking about power integrity by defining some of the problems that designers and engineers are facing?

Sam Chitwood: Power integrity has two different aspects, DC and AC. The first requirement is fundamentally supplying sufficient DC power to a device. Just like any mobile electronic

device you've used in the past, you must have a battery—a DC power supply. DC issues can stem from a combination of high currents and insufficient routing metal.

AC power integrity can be considered from both the frequency and time domains. In the frequency domain, we strive for a flat impedance profile across the bandwidth of interest. In the time domain, consider the example of many I/Os that are switching. If their power source isn't stable because it has a large amount of noise, that noise will manifest itself on those outputs as signal degradation. This phenomenon is known as simultaneous switching noise, or SSN, and shows how power integrity problems can cause signal integrity problems. Sigrity tools are special in that they can simulate signal, power, and ground together in both time and frequency domains.

Dack: Can simulation happen on the front end or the back end or both? Tell us where it's best used.

Chitwood: Historically, most power integrity simulations have been post-layout, towards



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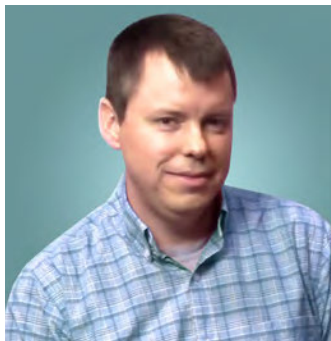
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the end of a design cycle. And obviously, that's where no one wants to be. Everyone is always running out of time, and there is almost never enough time to perform optimizations or a cost reduction. PI engineers barely have enough time to perform a signoff analysis to judge "pass or fail."

What we've really tried to do over the past two years is what my colleague Brad Griffin likes to call "shift left." That is, how can we move any type of analysis earlier—to the left—into the design cycle? Here is one example from a schematic point of view: Do you have enough decoupling capacitors on a rail? Do you have the correct decoupling capacitors on a rail? Most schematic designers today cannot answer those questions. Our goal has been to take what has historically only been done at the end-of-design cycle, a PI expert with barely enough time to do a check, and enable design engineers and layout engineers to assist much earlier. How can they participate?



Sam Chitwood

Dack: Upstream, to me, is meaning at possibly the schematic level.

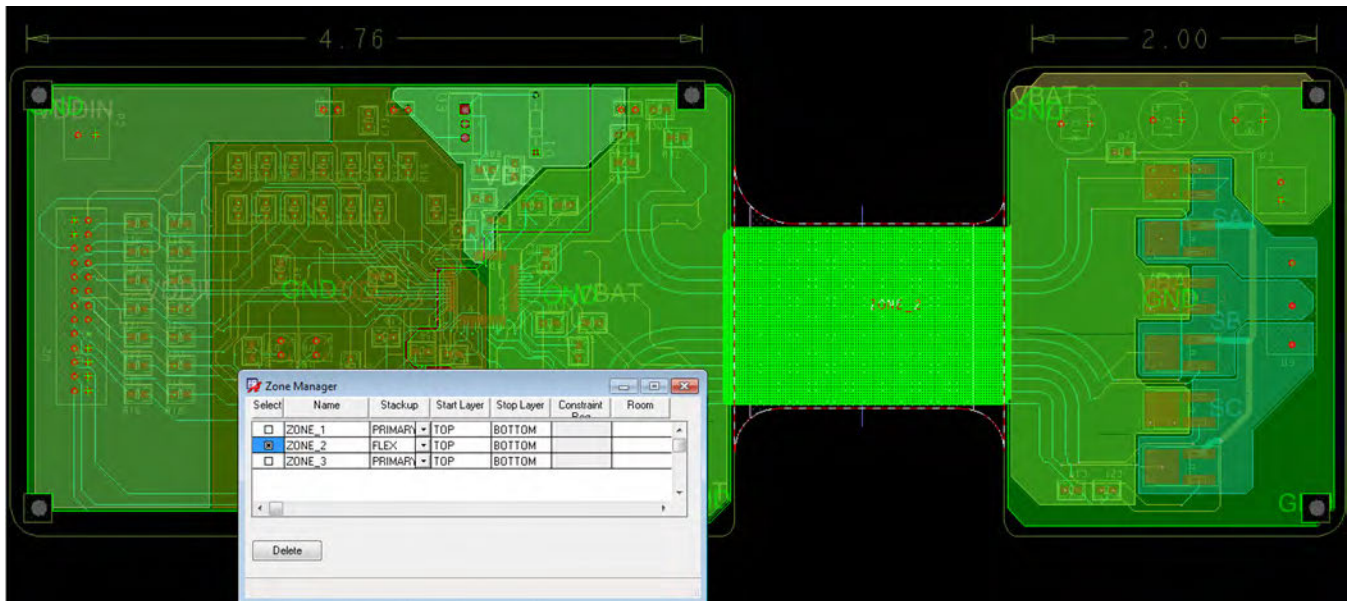
Chitwood: Yes, the goal is enabling schematic designers from the very beginning. This person needs an automated way of putting together something that is very simple and very quick but gives useful and actionable information. For example, have the correct decaps been selected? The schematic designer needs that information at the beginning, rather than have the PI expert at the very end say, "Oh, well, you had the wrong decaps all along." Now you have to go back and rip this out, and it can be as bad as literally starting over from your power delivery routing point of view. Obviously, that's tremendously expensive.

Dack: For the novice out there who might not be as educated in simulation as they may want to be, explain some of the elements of simulation, as far as parts and data sheets and what results we're looking for.

Chitwood: There is a great example of what we envision a layout designer being able to do who may be a novice at simulation. There are PDN inductance checks that we have made very easy to access. Absolutely no electrical models are required. All you need is the layout database with the correct stackup and the power net name of interest. With this information, the tools can automatically identify the component names and where they are placed. With respect to the IC device, we solve the loop inductance between the IC and each of its decaps. The objective is simple and the results are intuitive: Identify any decaps that are outliers. With specific problems identified, the layout designer can investigate if something has been improperly routed or if any decaps have been placed too far away. If so, do they need to be moved or switched from a top layer to bottom layer, for example. These problems can be quickly identified and corrected up front.

Dack: Upfront meaning not at the schematic level, right?

Chitwood: Correct, that example is for the layout designer. Now, let's shift-left to the schematic designer. As I alluded to earlier, the schematic designer needs to know what selection of decaps to choose from day one when no layout is available. What enables this flow is a PDN's target impedance. For an IC vendor that is providing a chip to a systems customer, we are advocating for these suppliers to also provide a target impedance so that the schematic designer can design to a specific level of pass-fail performance. Because without target impedance, the schematic designer is fundamentally stuck in a "better or worse" situation, where the designer says, "I can keep adding decaps, and I can continue making performance better, but when do I quit?" Without target impedance, there is no way to truly know when you are finished, no way to know pass or fail. This situation usually leads to significant decap overdesign and unnecessary BOM costs.



Dack: Yes. We get a target impedance, and we're using the tool up front at the schematic level. At what point can we determine if adding extra plane layers will enhance power integrity? Help us out. Tell us how the tool is used for determining stackup and planes.

Chitwood: For PDN stackup design, it's a great in-between area, between schematic and layout. We refer to this as pre-layout for a PDN.

Dack: Because we can add a layer just like that. How do we know how much that's going to help us to cost-justify for this?

Chitwood: PDN pre-layout is one of the workflows we have created to help guide users through selecting stackups and choosing PDN layer assignments. Performance can drastically differ whether you put a power plane near the top or bottom of a stackup, and whether you put decaps on the top or the bottom surface. Those are critical decisions that simulation can automate and also yields decap placement guidelines. Do not consider these results as mandatory decap placements at this stage, but as analytically-based suggestions. Three lists of decap recommendations are provided: decaps for the top layer, bottom layer, and underneath the device on the backside of the board. Given these three spreadsheets of pre-layout decap placement guidance, the layout designer now

knows exactly what to implement. This guidance is tremendously better than the previous rule-of-thumb guidance of "place decaps as close as you can to the device."

Dack: This gives the layout designer something to shoot for based on other target parameters in the design. For instance, a lot of designs are driven to strive for a single-sided assembly, so the designer will know the cost, already knows the cost of adding components and capacitors to the back side of the board as sole parts. But will he also know the performance gains and may become able to make a cost analysis?

Chitwood: Absolutely. One of the unique capabilities of our tools is the ability to include cost information as part of the decap optimization. It's not common, in these type of engineering tools, that you can study the tradeoff between electrical performance versus BOM cost. We can include the per-component cost, the assembly cost, and what is sometimes referred to as a BOM penalty cost (or the cost to stock that component during assembly).

Dack: A lot of the conversation among the attendees at this show is talking about high-speed and signal integrity issues, but we also have designers who are dealing with all the "design fors." We have "design for cost" parameters now. We have "design for manu-

facturability.” We talked about that, putting things one side of the board or the other. DFX, or “design for excellence.” Your tool is directly addressing cost.

Chitwood: Yes, directly from a decap BOM point of view and indirectly from a stackup and DC point of view.

Dack: Speaking of which, let’s cap it off with a discussion about DC. DC is huge.

Chitwood: To my knowledge, the Cadence Sigriety PowerDC™ technology was the first tool to combine electrical and thermal into one co-simulation environment, with literally one button-push where you get an electrical result and a thermal result, all within one GUI. That, as you can imagine, has been tremendously popular. For example, how many amps can be put through a specific via? How many vias are needed to move ten amps from one layer to another layer? Sigriety technology was the pioneer in this application.

Dack: That’s power-related and therefore thermal-related?

Chitwood: Yes, power and thermal are very much interrelated. I joke that you never want to see an email with the word “fire” in it. I’ve

seen customers have some creative ways of describing such a situation to their management. They may say that they’ve had, for instance, an “exothermal event.” Another good one is “light charring” of a PCB. But my personal favorite is “projectile vias.”

Dack: I haven’t heard of that. We used to talk about, “It’s OK if it gets warm, and it’s OK if it gets hot, but it fails when it lets the smoke out.”

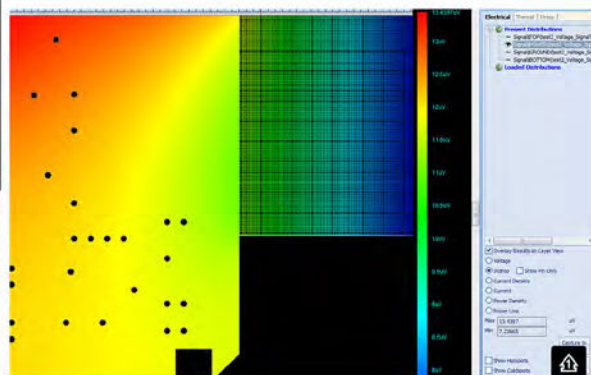
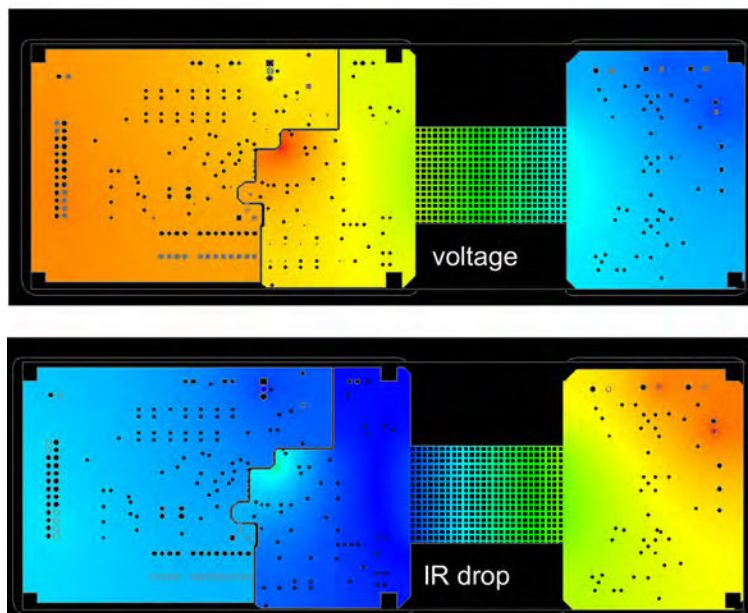
Chitwood: Agreed! We had a customer come to us specifically for this thermal capability because they had a cascade failure that melted vias out of their board. They thought they had sufficient number vias, but analysis showed the vias were not placed correctly.

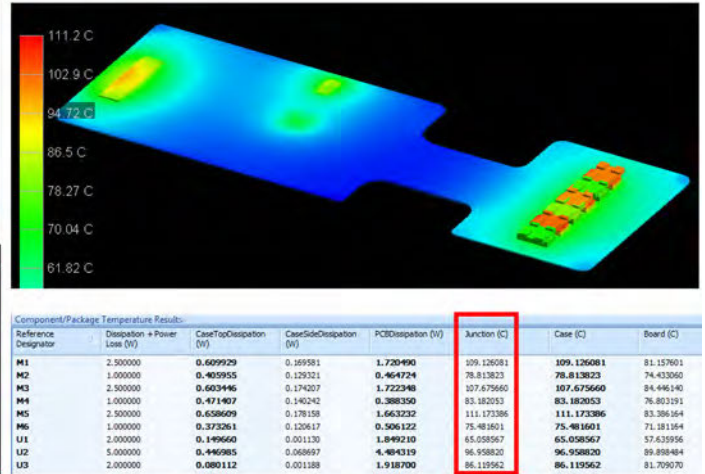
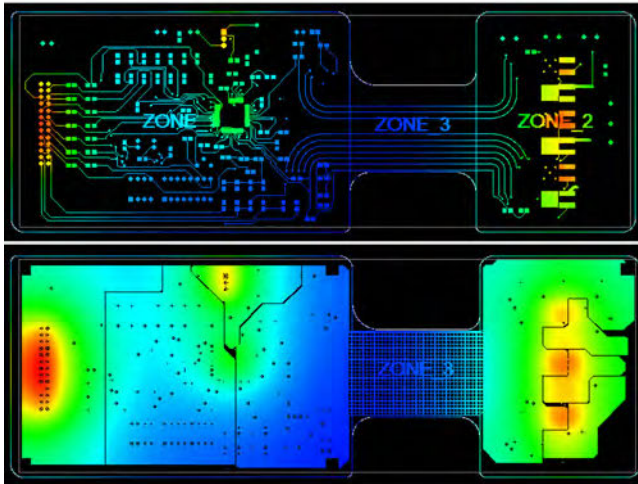
Dack: Circuit board materials aren’t typically manufactured or designed to handle heat. Heat is the enemy of circuit boards. Z-axis thermal expansion is just not good for vias anyway, regardless of whether they go projectile or not.

Chitwood: Let’s remember that the “FR” in FR-4 stands for fire-retardant, not fireproof!

Dack: Anything else you’d like to mention that we’ve missed?

Chitwood: Cadence has recently released new





power integrity utility technology, the Allegro PowerTree™ tool. This utility enables a new ecosystem of PI analysis to be shared between schematic designer, layout designer and PI expert. We want to truly automate the PI methodology in which all three of these users can contribute to PDN analysis that ultimately yields an optimized design within budget and schedule.

Dack: Tell us about the PowerTree tool and how it handles PI.

Chitwood: The objective is the ability to automate both DC and AC simulation setups and make things that used to be quite complicated now be extremely simple. For instance, a power domain on a large server board might be incredibly complex with dozens of net names associated with it. And these net names are not always human-readable, as in they are automatically generated and just random text strings. Obviously, a human doesn't want to track those names. The PowerTree tool automatically identifies all the DC nets from source to all loads. Components are automatically identified, such as any filter inductors, resistors, capacitors, their models are automatically assigned. Pass/fail constraints are automatically applied, such as per-pin voltage drop and target impedance. The simulations can literally be push-button automatic.

Dack: Wow. Sounds simple.

Chitwood: Yes, it is and from both a DC and an AC perspective. I'm sure you know that Cadence is famous for constraint-driven routing from a signal integrity perspective. We wanted to do the same thing from a power integrity perspective. We have many types of DC constraints and AC target impedance constraints. As long as these constraints are provided, PCB designers can have guaranteed correct power delivery from schematic all the way through the design cycle to board sign-off.

Finally, I will mention that we have an IC vendor here at DesignCon presenting this flow about how they are now providing target impedance to their PCB customers. We want to proliferate this methodology so that the rest of the industry can benefit from this flow.

Dack: Well, very good information, Sam. Thanks so much for your time today.

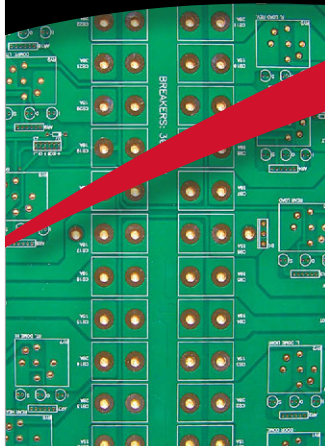
Chitwood: Thank you, Kelly. DESIGN007

Additional Reading:

1. [Sigrity Tech Tips.](#)
2. [How Your PCB Design Team Can Become Your PI Dream Team.](#)
3. [How a Team-Based Approach to PCB PI Analysis Yields Better Results.](#)
4. [Sigrity PowerDC Technology.](#)



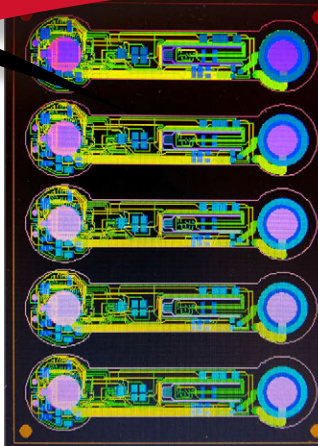
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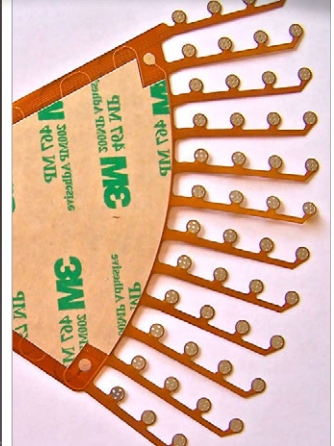
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Mentor's HyperLynx Automates SERDES Channel Design

by Andy Shaughnessy
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Mentor recently released the newest version of its HyperLynx signal integrity software. This version may be the first SI tool in the industry to fully automate SERDES design channel validation. I spoke recently with Chuck Ferry, product marketing manager with Mentor, about the new HyperLynx and some of the new serial link design capabilities that customers have been demanding.

Andy Shaughnessy: Some of the newer HyperLynx capabilities are focused on the users' SERDES design challenges. Part of the problem with SERDES seems to be that the standards for SERDES have been playing catch-up for a while, according to quite a few design engineers. What do you see going on in the SERDES standards space?

Chuck Ferry: SERDES-related standards have been evolving very quickly. The number of protocols for high-speed serial data has increased drastically in the last few years.

Often with each new generation of protocol, the data rates are doubling. Some of the challenges hardware designers face with the recent protocols are related to differences in the types of analysis that are required and the results they must understand to properly determine if a interface will pass or fail the requirements for that given protocol. For example, the new standards rely on new metrics such as channel operating margin (COM) to determine the pass or fail criteria of the interconnect.

Shaughnessy: What does it take to validate high-speed serial interface from chip-to-chip in a large system? It seems that it would be a real issue with a data center or cellular base station.

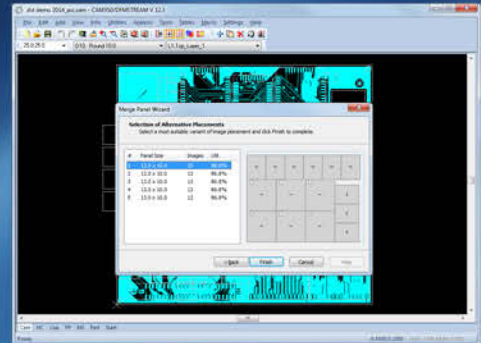
Ferry: To validate a high-speed serial link end-to-end per modern protocol every aspect of the signal interconnect between the chips must be modeled accurately including the IC packages, trace interconnect, as well as the characteristics of the drivers and receivers, including complex equalization schemes and optimization capabilities associated with those.

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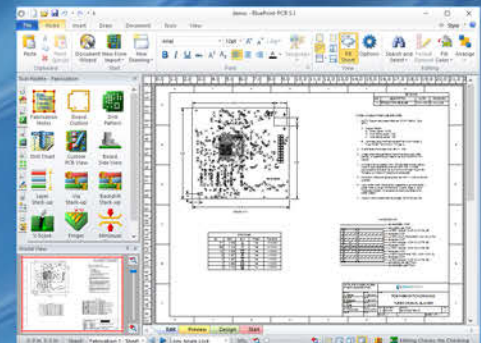
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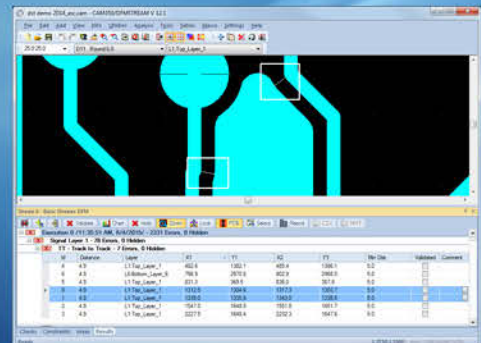
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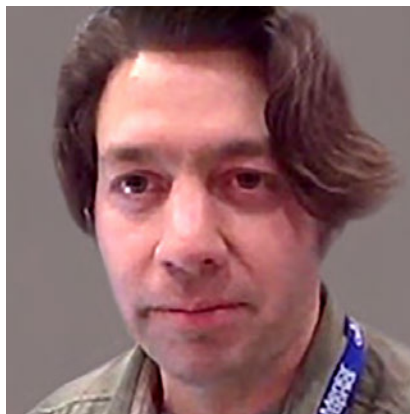
Shaughnessy: What questions are you hearing from hardware designers who are tackling these types of designs?

Ferry: The latest version of HyperLynx's new capabilities provides solutions to system-level designers with hard questions along these lines. They're wondering, "Are my implementations possible with various physical constraints and selected board materials? What if I don't have models for my driver or don't know what driver will be, but I just know the standard that it needs to comply to? How can I quickly validate an interface with this specific protocol standard? How can I model this long interconnect channel with 3D features in a reasonable amount of time? How can I find problems in my channel design before it's actually full routed?"

Our latest HyperLynx solution helps resolve and address these challenges by introducing the new interface compliance analyzer. As part of the solution we have embedded protocol expertise for the common protocols, over 25 are supported, including analysis and verification capabilities needed such as COM-based analysis for Ethernet, as well as built in protocol compliance models that can be used as alternative to IBIS AMI models. Including driver/receiver co-optimization capabilities for the protocol's specified equalization capabilities such as CTLE, FFE and DFE.

Shaughnessy: Are you doing anything to help the initial aspect of the design process before components have been selected and PCBs routed?

Ferry: To aid the up-front what-if analysis design phase, we have introduced the HyperLynx 3D Explorer which allows hardware engineers to easily create, solve and constrain common aspects of the interconnect that need to be solved with a 3D full wave solver. Users can easily select from a wide range of com-



Chuck Ferry

mon elements of the interconnect such as BGA breakouts, differential vias, series blocking capacitor configurations or connector pin fields, specify a range of parameters that will create a family of results (generated from a 3D full-wave solver) that are automatically measured against specified frequency domain mask and time domain constraints. This allows users an easy template based method to design the important building blocks of the high-speed channel interconnect with little advance solver knowledge needed.

Shaughnessy: How about the post-layout validation phase? Does this version address this aspect of the analysis process?

Ferry: For the validation phase, after the PCBs are routed, we've introduced new capability in HyperLynx that allows a fully automated channel decomposition approach. This solution intelligently scans channel interconnects of interest, decomposes them into different regions to be solved by optimal solvers. Some regions are optimally solved by 3D electromagnetic solutions and others in 2D solutions. This ensures that we have the capacity and performance to accurately solve long channel interconnects. The total solution, including the channel compliance analyzer, 3D Exploration capability, as well as the intelligent automated channel extraction really enables us to have the industry's best end-to-end high-speed series interface compliance solution in the market.

Shaughnessy: Sounds good. Is there anything else we need to cover?

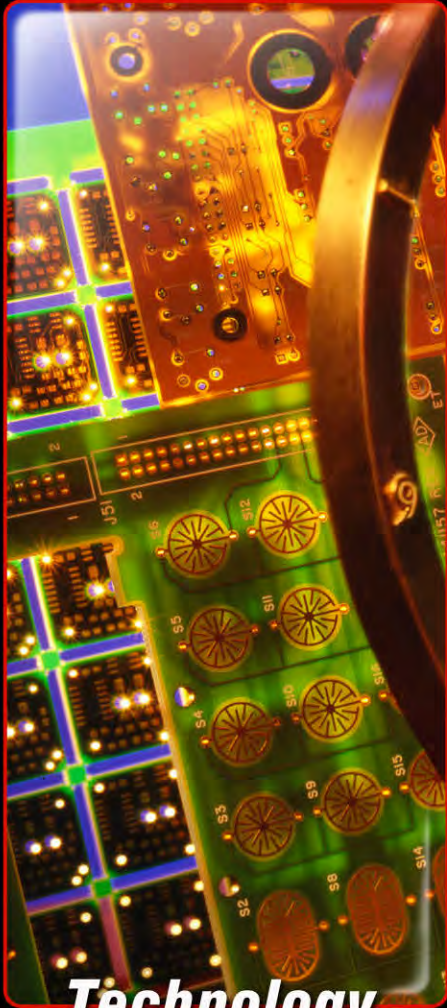
Ferry: I think that's everything.

Shaughnessy: Thanks for your time, Chuck.

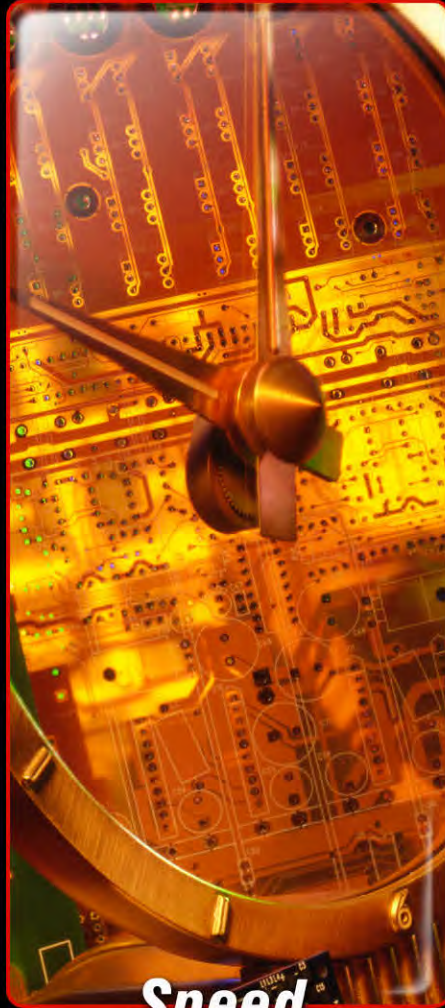
Ferry: Thank you, Andy. Always a pleasure.
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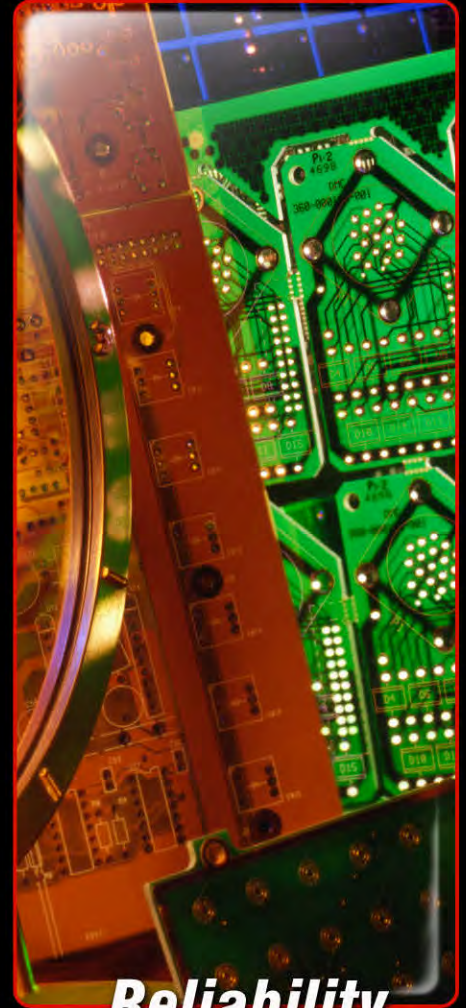
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Will Cool Technology Attract the Next Generation of PCB Designers?



Tim's Takeaways

Feature Column by Tim Haag, CONSULTANT

I'm loath to admit it, but my high-carb, high-fat, high-sugar, low-exercise diet plan is failing me, and I've got to make some changes in my life. OK, so my habits aren't quite as bad as that, but they aren't the best either. Meanwhile, my blood pressure has decided to do some aggressive stress testing of my cardiovascular system. It was so high at one point I thought that I might spring some leaks, so it is time to really focus on getting healthy and reducing some of these bad habits. I'm very sad to say my plan includes reducing my salt intake. Wow, eggs without salt are really...boring.

On the other hand, this problem has given me the opportunity to play around with some new technology. I purchased a blood pressure system that does all the work for me. It pumps the cuff up, measures my pressure and pulse, and then releases the pump. It will even average three measurements in a row to give me a

more exact reading, and it keeps an extensive record of my readings. On top of that, it also connects to my home network to transfer those readings. I must admit, I'm excited about this. Oh, sure, I'm still all jazzed up about my conversations with Alexa each morning to find out news and weather, and I love flying my Star Wars X-wing drone around the house. Additionally, there are also plenty of other high-tech devices around the house that are equally entertaining. But there's something about having a piece of technology in your hands that helps extend your life that makes it just a bit more enduring than the latest high-tech toy.

We live in an increasingly connected world. Ben Jordan of Altium recently theorized in these pages that there could be more than 200,000 new designs required to fulfill the needs of the [20 billion connected devices](#) projected to be in use by the year 2020. Yes, you read that



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correctly, 20 billion connected devices. To support the creation of all these devices will take a lot of work from PCB designers. Ben Jordan estimates that with an average of five design spins for each design, we are looking potentially at the completion of a million designs in the next few years.

Our industry needs more PCB designers to get this work done. Our numbers are dropping as designers are retiring, and we need an infusion of new designers and fresh ideas. Our industry is changing as well with more and more engineers taking on the entire task of design, from schematic capture to board layout, in what traditionally has been handled by multiple people. We need to find new ways to motivate younger people to take an interest in PCB design. Colleges, trade schools, and corporations are all trying different ideas to ignite this interest, but we still need more.

We need to find new ways to motivate younger people to take an interest in PCB design.

Over the years, I've designed a lot of different boards that have served various functions. Some went into products that I was unaware of, and I was not permitted to know the final product of quite a few of them. In one case, a team of mysterious men all dressed alike came to our service bureau and sat in the conference room for a week drinking coffee while we designed their boards. Once the designs were finished and they had approved them, they disappeared stealthily into the fog of the night. They came from a very well-known high-tech company, which I won't mention by name, and they behaved as if they owned the world. Perhaps they did and I never got the memo, but in any event the mystery that surrounded them and their matching suits was very reminiscent of "Men in Black," and that was before

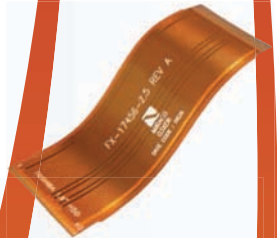
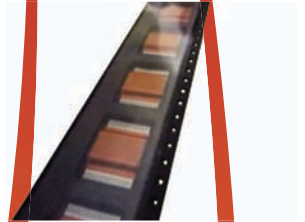
the movie even came out. I didn't want to ask them what the boards were for because frankly, I didn't want to hear them say "We could tell you, but then we'd have to kill you."

However, I have known what most of the circuit boards that I've designed through the years were for. I've always worked hard to give every PCB design job my very best effort, as I know that all of you have too, but I have discovered something and I wonder if any of you have discovered this as well. Those boards' functions that were interesting to me were the boards that I had the most interest in designing. I guess that this is probably normal human nature at work. For instance, I've designed huge power delivery boards for industrial power panels (snooze), that I couldn't wait to get through with. I've also designed lots of simple test-type extender cards (yawn) that paid the bills. The cool stuff though, oh yeah baby! Those were the designs that I lived for.

I designed some of the first touch-screen panel boards, and video boards for computers. Those were great because I could tell people what I was doing and their eyes wouldn't glaze over as fast as normal. I also have designed system boards for display products, which was awesome because I got to take some of those products home and use them for watching movies with my kids. That earned me some big points in the "My dad has a cooler job than your dad" department. And then, as the coup de grâce, I designed some of the early mother boards for personal computers. After telling that to my friends and family, I got hailed as the guy who was responsible for the new personal computers of the day. I must confess though, I may not have corrected that misconception quite as fast as I really should have to bask in the glory for a while.

It's easy to have a higher level of interest in what we are designing when those designs have a direct impact on our lives. Many years ago, I designed a small board for a wearable product. At that time, the phrase "wearable" hadn't been coined yet, but that's what it was for. This was towards the beginning of that genre of products, and now we are seeing this field explode with all sorts of different devices.

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It was only natural that eventually these products would need to communicate with other products, and they soon joined the ranks of connected devices. The entire arena of connected devices has become so huge now that it is mind-blowing in scope.

Perhaps the key is to get people interested in creating and designing those technologies that are important to them. At this point in my life I can honestly say that if I had the opportunity to design some boards that went into medical detection equipment like my new blood pressure cuff, I would be extremely motivated to do that. Maybe what we should be focusing on is not just playing with the new toys, but showing the younger generation different ways to think about how they can improve upon these new toys. It's something to consider anyway.

And with that, it is time for me to wrap up my arm once again and do another BP check. If one of you designed the electronics for this wonderful gizmo that is monitoring and helping me control my blood pressure, I want you to know how grateful I am to you, and I say that in all seriousness. Please keep up your great designing, and let's all work together at getting more people joining us in what we do.

DESIGN007



Tim Haag is a consultant based in Portland, Oregon.

Scaling Silicon Quantum Photonics Technology

An international team of researchers led by scientists from the Uni. of Bristol's Quantum Engineering Technology Labs has demonstrated the first ever large-scale integrated quantum photonic circuit, which can generate, control and analyze high-dimensional entanglement with unprecedented high precision and generality. The quantum chip was realised using a scalable silicon photonics technology. The work, in collaboration with Peking Uni., Technical Uni. of Denmark (DTU), ICFO - The Institute of Photonic Sciences, Max Planck Institute of Quantum Optics (MPQ), Polish Academy of Sciences (PAS) and Uni.

of Copenhagen, has been published recently in the journal Science.

Significant progress towards large-scale quantum systems has been recently reported in a variety of platforms including photons, superconductors, and ions, among others. In particular, photonics allows a system to naturally encode and process multidimensional qubit states within a photon's different degrees of freedom. In this work, a programmable bipartite path-encoded multidimensional entangled system with dimension up to 15×15 is demonstrated, where each photon exists over 15 optical paths at the same time and the two photons are entangled with each other there.

Professor Mark Thompson, leader of the Bristol team, has emphasized that "the photonic circuits on silicon, the same material used in our electronic circuits, allow the processing of information carried by a single particle of light. This silicon quantum photonics technologies are allowing us to scale up quantum devices and systems in an incredibly rapid speed, and in the near future it will reach an integration of tens of thousands of elements on a single chip that can promise numerous quantum applications."



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SnapEDA Harnesses Technology to Provide Verified Parts

by Andy Shaughnessy
I-CONNECT007

Like many young entrepreneurs, Natasha Baker knew she wanted to run her own company years before she finally pulled the trigger. But she waited until the time was right, developed a business plan, and stuck to it. Now, five years after SnapEDA was launched, the company continues to expand its library parts and symbol creation services, with the help of some of today's most cutting-edge technology. I caught up with Natasha, and we discussed how her team utilizes technology that has helped SnapEDA to become a major player in this space.

Andy Shaughnessy: Tell us a little about your company.

Natasha Baker: Sure. SnapEDA is a website used by half a million hardware designers globally to build their circuit boards faster. We provide the building blocks needed to bring designs to life, such as the symbols, footprints, and 3D models.

When we launched in 2013, the problem we set out to solve was, "How can we remove barriers in the design flow so that designers can innovate faster?" We saw that content was a huge opportunity for this, since designers spend days making models for each component on their circuit board from scratch, or were skipping potentially beneficial aspects of design, such as simulation, due to an inability to find simulation models.

The problem came to a head when I was making a circuit board for a trade show that ended up taking triple the amount of time it should have due to a lack of content in my design tool.

I thought, "What if we could create Google for circuit board design? It would be a place that provides designers with ready-to-use content, and transparency into the quality of that content." And that's how the idea for SnapEDA was born.

Since we first raised funding for the company two-and-a-half years ago, our community of electronics designers has grown over 4,000%, and our monthly growth continues to accelerate. Our users love it because it's high quality, fast, and easy-to-use.

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It's also entirely free for designers. We don't limit the downloads, and there's no prompts to upgrade. This is because, as a team of over 20 passionate engineers, we built the product we would have wanted. We're able to do this by working with component vendor and distributors.

Shaughnessy: What is your latest news?

Baker: Our latest news is that we've collaborated with TE Connectivity, a \$13 billion leader in connectivity and sensors. In February, we launched over 25,000 new CAD files for their products on SnapEDA, including connectors, relays, switches, sensors, and more.

I'm also excited to announce here that TE Connectivity will be sponsoring our InstaPart service for a limited time. For those who are unfamiliar, InstaPart is our 24-hour symbol and footprint request service. Although SnapEDA is free, sometimes engineers need parts quickly that aren't yet in our library. Once we add the part, it's made available to the entire community to download for free.

With TE Connectivity sponsoring our InstaPart service, engineers can now special request complex connectors and other electromechanical components and sensors produced by TE Connectivity in 24 hours for only \$9. We know this will save engineers a lot of time, while also helping future engineers who might need to design with that component.

Shaughnessy: The logistical aspects of what you're doing, basically revolutionizing how library parts are managed, seem daunting. Are you all writing your own software for this?

Baker: All our software is developed right here in San Francisco. Every day, we deploy code



Natasha Baker

that keeps improving the product based on feedback from our community, whether it's to the website, API, or our EDA plug-ins. We're also constantly writing new exporters. Right now, we support Altium, Allegro, OrCad, PADS, DXDesigner, PCB123, and KiCad, and plan to add more this year.

Shaughnessy: What kind of new technologies have you implemented, or do you plan to implement?

Baker: We are taking a completely fresh approach to solving the content problem. One big differentiator, is that we focus on automation to bring quality and scale to our parts creation and verification processes.

For parts creation, we built an awesome new (free) computer-vision symbol creator called [InstaBuild](#). Designers simply highlight the pin-out table, and our technology automatically configures the symbol based on our standards and maps it to a verified, IPC-compliant footprint.

When it comes to parts verification, our team is laser-focused on nailing the quality issues that have plagued other sources of content. For example, we created a real-time CAD model quality scanner. When viewing a CAD model on SnapEDA, we run through over 30 quality checks on each CAD model and show the results of these checks right on the page. Things like whether the centroid is defined in the correct place, or whether there is silk-screen overlapping any copper pads. We also show whether the part was made with IPC standards, or the manufacturer's recommendations. We distill this information into a "report card" that can be viewed instantly. This way, the designer can trust in the content, and be aware of any limitations it might have for their application.

We also have plug-ins. Designers can download a plug-in for their EDA tools so they can search parts right within their design environment, PCB123, a free design software tool provided by Sunstone Circuits, can even search the SnapEDA library pre-installed within it, which has been very successful.

We have a ton of other cool stuff on the site, such as the ability to create your own library which can be batch downloaded in one-go. Our team is obsessed with creating cool easy-to-use technology, so I'd invite any designer reading this to check out the website.

Shaughnessy: When you look at our industry overall, what new or recent technology really impresses you?

Baker: Lately I've become fascinated by the aerospace and space electronics being created by smaller companies. We have designers using SnapEDA to build everything from fully electrical airplanes, to satellites, to rockets. In the past couple years, we've seen this trend towards tiny startups creating these types of devices, and I think that's absolutely incredible. It has also gotten me really interested in the challenges of space electronics which are very nuanced when it comes to component selection.

Shaughnessy: What is SnapEDA working on over the next few years?

Baker: We have a great roadmap ahead in terms of free tools that will continue to make the design process easier. And of course, our roadmap is constantly being shaped by our community. If you want to be a part of this new paradigm around design content, please check out our [website](#).

Shaughnessy: Thanks for speaking with me, Natasha. Sounds like a great time for your company.

Baker: Thank you, Andy. My pleasure. DESIGN007

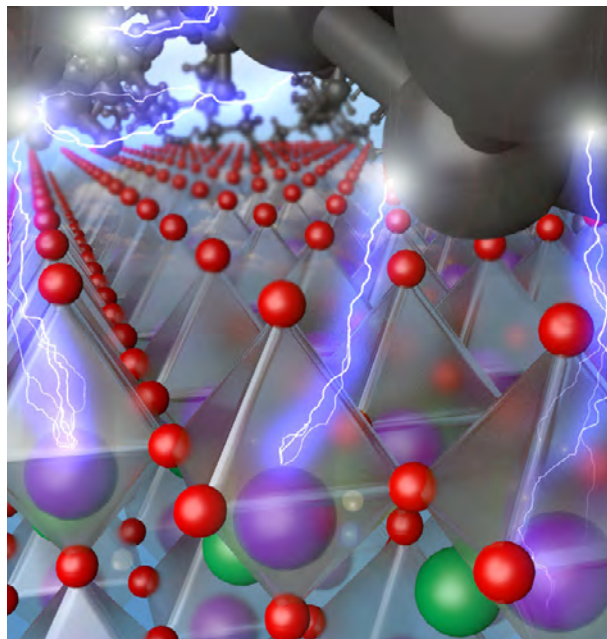
New Transistor Concept, Solar Cell Included

ICN2 researchers have developed a novel concept in transistor technology: a two-in-one power source plus transistor device that runs on solar energy. Published in *Advanced Functional Materials* and currently trending in the Wiley-VCH "Hot Topics" list, lead author Amador Pérez-Tomás is calling it the "solaristor."

Transistors are everywhere in modern electronic devices. Where wires transport electricity from A to B, transistors can modulate the current between high and low states which, translated into sequences of 1s and 0s, is the basis of the age of information.

But your phone needs more than transistors to work; it also needs an energy source. All electronic devices are connected up to a battery of some kind, requiring cables, sometimes complex systems and a lot of space -the battery is the single biggest component of any mobile phone. What ICN2 researchers propose in this work is a compact self-powered transistor that incorporates the energy source and the transistor into the same slim unit. What's more, the energy source is the Sun.

This game-changing concept combines the best of solar cells and the best of transistors into a single device the size of a biological cell.





Estonia a Hot Spot for New Technology

Self-driving buses were introduced in Tallinn, Estonia in 2017 for a trial period.

by **Andy Shaughnessy**
I-CONNECT007

If you're in the electronics industry, odds are that you use Skype every day to connect with people from around the world. Did you know Skype was founded in Estonia? Most Westerners know very little about Estonia. A former Soviet Bloc country, Estonia has come a long way since restoring its independence in 1991. Electronics companies are thriving in this tiny EU member country, and capital city Tallinn has been called "Silicon Valley on the Baltic Sea." During productronica, I met with Arno Kolk, general manager of the Estonian Electronics Industries Association, and we discussed the explosion of new technology in this "Baltic Tiger" country?

Andy Shaughnessy: Arno, nice to meet you here at productronica. Please begin with a little background about the association.

Arno Kolk: Well, it's a voluntary association. It's quite typical, I would say. In this association,

the companies work together to improve cooperation and have closer ties with universities, which are receptive of the solutions, and then we increase the productivity of all the members.

Shaughnessy: What is the manufacturing atmosphere like in Estonia, and what sort of industries are found there?

Kolk: In Estonia, the manufacturing industry plays a very important role. Our industry share of GDP is on par with the rest of Europe. I think most of Estonian exports, about 80% of exports, is manufacturing, and electronics is over 20% of Estonian exports. Being a small country, the local market is tiny, so we must export. It also means we must be competitive with exports. But then I guess your readers don't know that the Estonian industry goes back a century or more, and the electronics industry is as old as electronics. We had our first telephone factory back in 1907.

Shaughnessy: I'll bet I'm not the only person who wouldn't have guessed that. And the

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industry has continued to stay relevant since that time?

Kolk: Yes, we built radio sets in the '20s and it grew from there. Of course, we had at least 50 years of Soviet occupation where electronics was present and thriving, but it was behind Iron Curtain, which means it was really tailored to that market. When the wall came down, we were out in the cold, because that was our competitive market and we were not part of the global value chain. We perhaps used different processes and different approaches, so we had to learn—very fast.

So we had a complete industry overhaul in the '90s, and now I'd say we are world class, as our export figures show.



Arno Kolk

We have large multinationals, the biggest of them being Ericsson, who has a large factory in Estonia, and American companies, FLIR, Amphenol there and others. Then we also have EMS companies, usually European middle-sized companies. And then we have an increasing number of engineering companies that are really growing. Some of them are exporting just engineering services, and others develop complete products while some companies launch their own products. So we have the whole value chain in place: design companies, several manufacturing companies, after-sales companies, and all the major distributors are present in Estonia, so the components can be bought locally. Likewise, all the machinery, all the materials, all we need for electronics manufacturing is there.

And Estonia is now rather famous for our IT companies and how well IT is implemented in government services. Citizens communicate with the state through the Internet. So now we are basically marrying this together with our industry and all that came before. Everything is growing nicely.

For our electronics industry and especially for engineering companies, we see a large opportunity in helping companies make their products smart and connected. That's what it's all about now with IoT and all these things. You really cannot sell a product today that is not connected and doesn't have an app with it. Our electronics engineers and IT guys together can create the complete solution to help companies in very different sectors, be it smart clothing, smart cities, or smart machines. We are about to have very interesting references there. I will gladly work with American colleagues in the same way.

Shaughnessy: You talked about being able to compete on the global market and keeping your cost down. What's the secret to doing that?

Kolk: Well, we cannot really be the cheapest. There is always somebody who can undercut you by five cents. Although now we have cases where we have done competitions with factories in China and India, and we have better pricing because of a more streamlined production and better organization. But we don't have many people, so we have to manage with small teams and do big things. And it shows in the price at the end of the day.

Another thing is that the local market is small and we are not the cheapest place in the world, so we don't produce too much consumer stuff anymore. We used to make cellphones in large volume in the old days, but now it's mostly professional electronics. So, we're talking about automotive, railway, aerospace, industrial. These are industries where the quality, reliability and the delivery matters.

Shaughnessy: Doing the high-tech stuff.

Kolk: Doing the high-tech stuff, yes, and you have to be close to the customer, so we are serving Northern Europe, Scandinavia, Germany, and these areas. We are close and we can get products over there by truck in day or two. It works pretty well.

Shaughnessy: Tell us about your background.

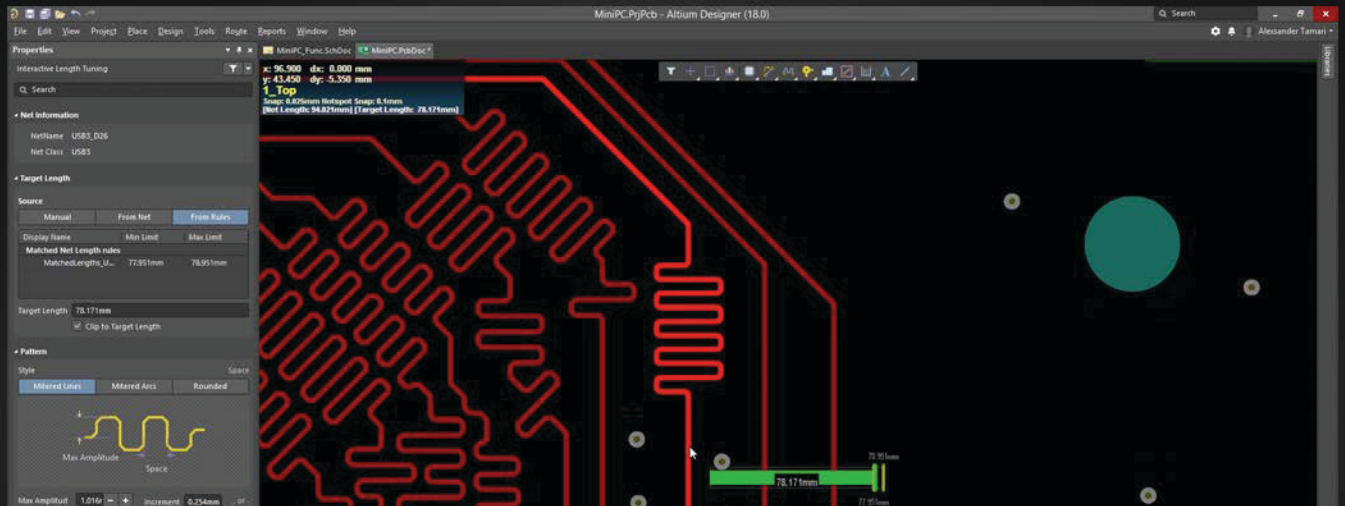


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Kolk: I started at the university in R&D, then I moved to engineering companies and spent 15 years at EMS companies in different parts of world.

Shaughnessy: Is there anything else you would like to talk about? I think Americans need to know more about this part of the world.

Kolk: Again, in IT, we have many success stories in Estonia. Skype was first developed in Estonia, for instance, and there are now more unicorns (private companies worth \$1 billion) coming up, so we try to repeat the same success in electronics as well. There are some rather promising young companies now. For example, there is one company called Skeleton Technologies. They have developed some supercapacitors that are record breaking. They have one factory in Estonia, and they have built a new one in Germany for all the automotive and aerospace business.

There are some other crazy things now on the boundaries of different sectors. For example, an Estonian company called Starship Technologies is making delivery robots. These are small, six-wheel things which drive on a sidewalk amongst the people, and they can cover

the last mile for delivery, be it pizza or personal parcels, or something like that. And it's fully autonomous, so it finds its own way. Now they are cooperating with German automotive industries so that they can have a small minivan to serve as a base for these guys. The minivan stops in the middle of a city block, and then these small robots swarm out and deliver parcels. Then they go to next block. They call themselves a logistics company. I call them an electronics company because they have complex electronics and processing inside.

Shaughnessy: If it can drive down the sidewalk among crowds of people, it must have sonar.

Kolk: It has sonar and a bunch of cameras and lot of real-time processing.

Shaughnessy: That's fascinating. It sounds like a good time to be in electronics in Estonia.

Kolk: Absolutely.

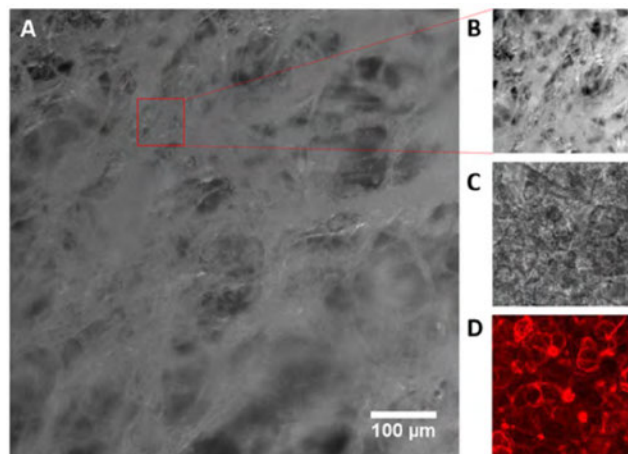
Shaughnessy: Thanks for your time, Arno.

Kolk: Thank you for the opportunity, Andy.
DESIGN007

More Realistic and Accurate Organs-On-Chips

In a step toward better diagnosis and treatment of digestive conditions, such as inflammatory bowel disease, scientists report in *ACS Biomaterials & Engineering* that they have developed a first-of-its-kind collagen-based membrane for use in microchips.

Recently, researchers developed a way to grow living cells in microfluidic chips. Commonly called an organ-on-a-chip, each device is typically composed of a pair of flexible, translucent polymers or plastics that surround a porous membrane.



The researchers produced three types of microfluidic devices. One had no membrane, and the second had a plastic-derived membrane. For the third device, the research team used collagen to form the membrane. Then, they placed human colon cells in each device. The researchers concluded that using collagen-based membranes in organ-on-a-chip devices enhance the growth, viability and barrier function of human colon cells and that the method likely could be extended to cells from other organs.



2018 Programs

February 24–March 1

San Diego, CA, USA

IPC APEX EXPO 2018

March 1–2

San Diego, CA, USA

The Pb-Free Electronics Risk Management (PERM) Council Meeting No. 35

IPC APEX EXPO

March 20

Tempe (Phoenix), AZ, USA

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March 20–21

Tempe (Phoenix), AZ, USA

IPC Technical Education

Day One: EMI Control-Grounding, Power Distribution, Board Stack-up and More

Day Two: Practices to Produce a More Manufacturable Board and The Complexities of Fine Pitch BGA Design

April 10

Boston, MA, USA

IPC Day

Complimentary event, network and learn more about IPC

April 10–11

Boston, MA, USA

IPC Technical Education

Day One: IPC Technical Education — PCB Fabrication Basics: Process and Specification

Day Two: IPC Technical Education — Advanced Troubleshooting

April 16–17

Ingolstadt, Germany

IPC Europe Technical Education

in English

April 18–19

Ingolstadt, Germany

IPC Europe Technical Education

in German

April 24

San Jose, CA, USA

IPC Day

Complimentary event, network and learn more about IPC

April 24–25

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IPC Technical Education

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May 2

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IPC Technical Education — PCB Layout — Place and Route

In conjunction with Del Mar Electronics and Manufacturing Show

May 8

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Afternoon: IPC/WHMA-A-620 CABLE & HARNESS DOCUMENTS: The Evolution of IPC's Cable and Harness Documents – A Brief History

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PCB007 Highlights

Failure Analysis: A Critical Component to Process Engineering ►

My definition of process engineering: attempting to put together the perfect manufacturing stages to produce the desired product. Printed circuit production includes many diverse production stages.

I-Connect007 Launches *Fundamentals of RF/Microwave PCBs* Micro eBook ►

I-Connect007 is excited to announce the release of the latest title in our micro eBook design series: *The Printed Circuit Designer's Guide to... Fundamentals of RF/Microwave PCBs*.

All About Flex: Polyimide vs. Silicone for Flexible Heaters ►

Flexible heaters are sub-divided into two primary technology platforms: etched-foil and wire-based technology. Wire-based (wire strands woven together or single strand wire) is the more common technology, with multiple customers offering a wide range of products.

Equipment/Process Selection: Case Study of a DMADV Approach to PCB FAB Process Design ►

This article outlines the approach we took to designing this new phase of our commercial existence, which has now been spun off as a separate business unit known as GreenSource Fabrication.

EIPC's 2018 Winter Conference in Lyon Review of Day 1 ►

Venue for the 2018 EIPC Winter Conference was the splendid new Alstom Transport Information Solutions facility in Villeurbanne, in the Lyon metropolitan area of the Auvergne-Rhône-Alpes region in Eastern France.

The Best It's Ever Been, Every Year: The Goal for IPC, Part 1 ►

The end of 2017 caps an exciting time for IPC and IPC China as membership has grown substantially, in part because of new offerings from the organization to its Asian members. John Mitchell and Phil Carmichael discuss IPC's focus for 2018.

Solder Limits: Updates for the Age of Surface Mount ►

Solder limits are one of the fundamental parameters used when evaluating the PCB, solder resists, and metal-clad base materials for safety under the UL Recognition programme.

All About Flex: Copper Thickness Requirements for Flex Circuits ►

An end user will specify the copper thickness of a printed circuit for different reasons. The most obvious reason would be for current-carrying capacity, but copper thickness also directly impacts thermal performance and impedance.

CircuitData: Creating an Open Source Language for PCB Data Exchange ►

I recently spoke with Elmatica CTO Andreas Lydersen on a subject of great interest, namely CircuitData. This open source language promises to greatly improve the communication of details that can be misinterpreted.

Willy Wonka: The Lean Case Study ►

No matter where my travels take me, I hear a wide and limitless supply of excuses for why Lean will not work in "my" organization. One of my favorite ways of illustrating that Lean will indeed work anywhere is to take a Lean look at Willy Wonka's Chocolate Factory.



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AC/DC is not Just a Rock Band

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Positioned at our usual table, directly in front of the stage at the local pub in Melbourne, Australia one Friday night in 1972, the boys and I laughed as a school boy, guitarist Angus Young, set up equipment and tuned a guitar. We assumed he was just one of the roadies, and were gobsmacked when the band unexpectedly fired up. High-voltage is not the word—more high-wattage, deafening—you could feel the sound as your ears distorted. The slick, gritty, blues-based lead riffs of the budding guitarist were insane. Little did we know that AC/DC's raucous image, with wild solo riffs, would make them one of the world's top heavy-rock bands. We willingly endured this every Friday night for weeks on end. Fortunately, the venue

was also a target-rich environment of eligible young ladies. In this month's column, I will discuss AC coupling (or is it DC blocking?) of high-speed serial links as my taste in music has matured over the years.

SERDES (serializer/deserializer) serial links are used to provide high-speed, high-bandwidth data transmission over differential signals and minimize the number of I/O pins and interconnects. And although it saves the PCB designer routing numerous parallel traces, implementing high-speed serial links can be challenging. Any small discontinuities in the physical geometries, along the transmission path, can significantly degrade the signal. This degradation includes loss of amplitude, reduction of



Figure 1: AC/DC fires up at an early gig (source: Kat Benzova).

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| Product | Thickness | Thermal Conductivity (Z-Axis), W/mK | Thermal Impedance, C-cm ² /W | Tg, C | CTE (Z-Axis), ppm/C | | Dk, 1MHz | Df, 1MHz | Breakdown Voltage, kVAC | Flammability |
|---------|-----------|-------------------------------------|---|-------|---------------------|-----|----------|----------|-------------------------|--------------|
| | | | | | <Tg | >Tg | | | | |
| 92ML | 8mils | 2.0 | 0.52 | 160 | 22 | 175 | 5.2 | 0.013 | >50 | HF V-0 |

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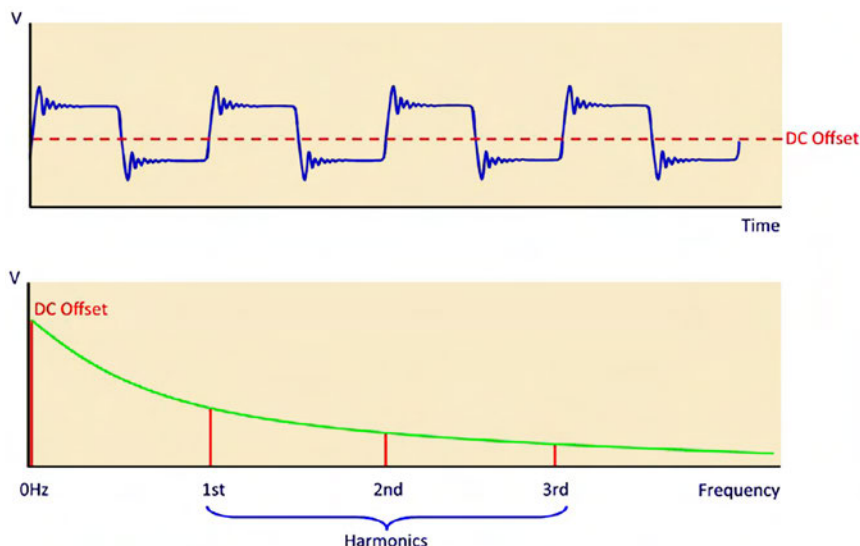


Figure 2: AC and DC components of a signal transferred to the frequency domain.

rise time, and increased jitter. As a result, one must be able to identify these discontinuities, in the high-speed channel, and mitigate their impact to improve the performance of the signal transmission.

A capacitor is typically placed in series with both differential signal traces to remove common mode voltage differences between ICs or different technologies. An “AC coupling capacitor” or “DC blocking capacitor” basically refers to the same thing. Any capacitor placed in series with the signal path tends to pass the high-frequency, AC portions of the signal, while simultaneously blocking the low-frequency DC portions. Since these capacitors couple transmitter to receiver, I prefer to use the term “AC coupling.”

In Figure 2 (top), the signal fluctuates about the DC offset. After performing a Fourier transform on a signal that consists of both AC and DC components, the DC component will be at 0Hz and the AC signal will be at its associated harmonic frequencies (bottom).

AC coupling is useful because the DC component of a signal acts as a voltage offset, and removing it can increase the resolution of the signal and allow different technologies to communicate without level shifters. Level shifter ICs can otherwise provide an interface between components that operate at different voltages. However, level shifters introduce delay varia-

tion (skew), increase power consumption, and are not suitable for low supply core voltages. AC coupling is needed to maintain the correct DC bias for receivers. If the transmitter has 0V DC bias and is of the same technology, then AC coupling does not have to implement.

The most important parameter, of the AC coupling capacitor, is the relative geometry with respect to the substrate. The capacitors are placed in series with high-speed traces and as such, the capacitor body becomes a section of transmission line. The equivalent series

inductance (ESL) of a capacitor, critical for bypass and decoupling applications, becomes negligible for AC coupling applications because the transmission line has inherent inductance anyway. Instead, the thickness of the stackup outer dielectric, trace width, land size, solder thickness and cover-layer thickness of the capacitor all interact together in the area of the capacitor.

In a well-matched interconnect, it does not matter where an AC coupling capacitor is placed. What does matter is how well the capacitor transition is designed, how low the reflectivity is, and whether it is placed near other channel discontinuities. Far away from other discontinuities is best.

AC coupling removes the common mode level and allows the receiver to set its own bias point. This is especially useful for rack-to-rack systems where the common mode cannot be well controlled. It also has the advantages of allowing:

- VTT referenced and GND referenced systems to work together
- A single SERDES channel to cover multiple standards
- Newer (restricted supply) devices to work with legacy devices
- The ability to hot-swap and protection from external shorts

However, AC coupling capacitors are common sources of impedance discontinuities in high-speed serial channels. Typically, narrow trace width and close trace spacing are used to construct the 100Ω differential transmission line pair. However, as these narrow trace pairs are routed into the surface mount lands of a capacitor, the sudden widening of the copper, as they join with the capacitor lands, causes an abrupt impedance discontinuity. The effect of this discontinuity appears as excess capacitance because the surface mount lands, of the capacitors, act as a parallel plate with the reference plane beneath.

To eliminate the excess parasitic capacitance, associated with surface mount lands, a portion of the reference plane, that is directly beneath the component, should be removed. This allows the signal that traverses through the capacitor

to reference a lower plane (further away) and reduces the parasitic capacitance, thereby minimizing the impedance mismatch. This principle should also be applied to surface mount connectors if present in the path (Figure 3).

On the left there are two capacitors which are referenced to the plane on layer 2. Whereas, the picture on the right shows the optimized structure with the plane cut outs included. The lands then reference to the layer 3 plane increasing the impedance. The board stackup and trace geometries (Figure 4) are designed to provide a 100Ω differential signal. All traces and plane layers are 1 oz. copper. The width of the surface mount lands is set to 20mils to match the width of the 0402 type capacitors. And, the length of the cut out is equal to the end-to-end distance of the two surface mount lands. The iCD Stackup Planner can be used

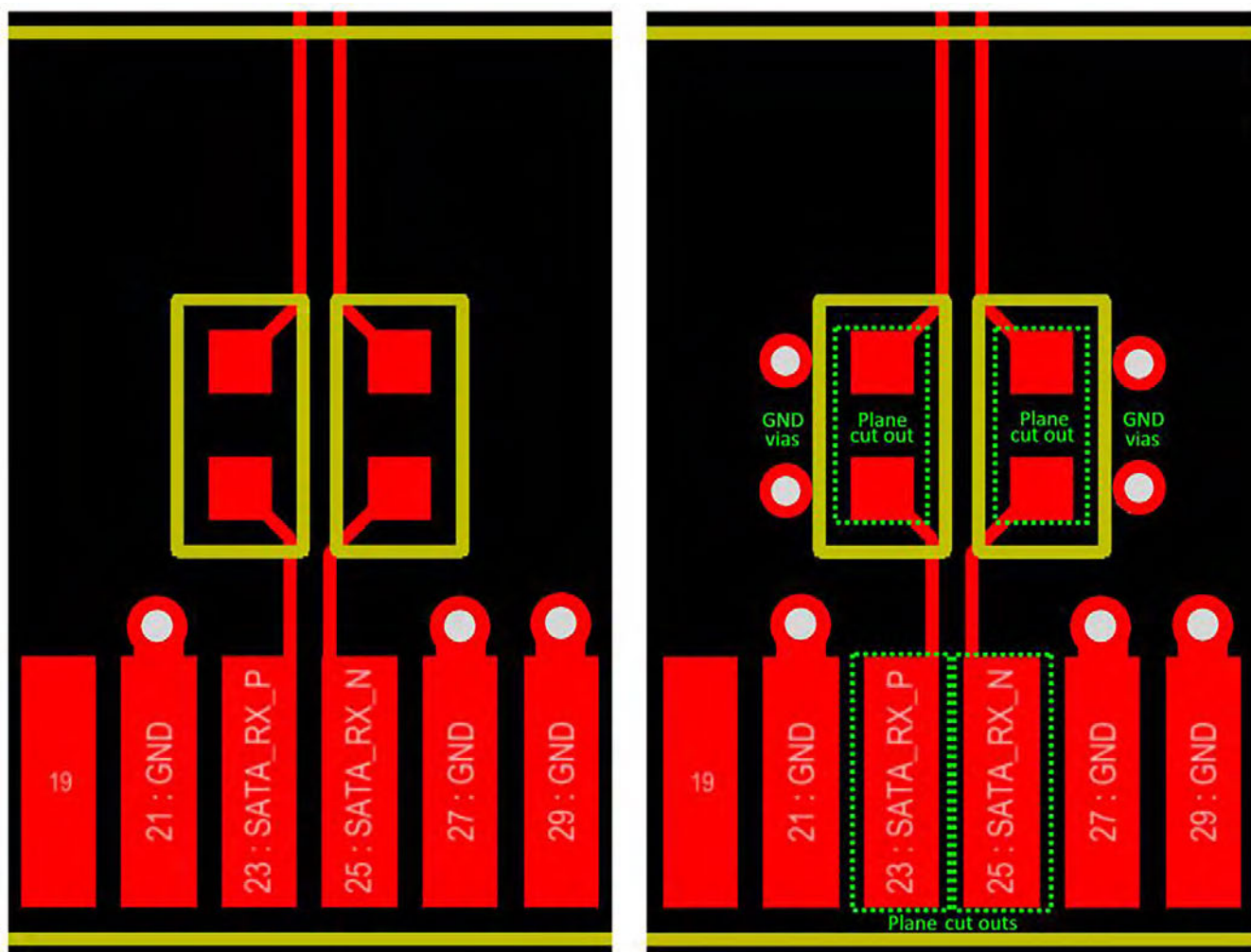


Figure 3: AC coupling capacitors (left) with plane cut-outs and GND vias (right).

| Stackup Planner PDN Planner CPW Planner | | | | | | | | | | | | | |
|--|-----|-------------|------------|---------------|---------------------|----------------------|------------------|-----------------|-------------|----------------|-------------------------------|-----------------------------------|---------------------------------------|
| 2 Layer 4 Layer 6 Layer 8 Layer 10 Layer 12 Layer 14 Layer 16 Layer 18 Layer 12 Layer addc | | | | | | | | | | | | | |
| UNITS: mil 2/5/2018 Total Board Thickness: 61.4 mil | | | | | | | | | | | | | |
| Differential Pairs > 100 ohm Differential | | | | | | | | | | | | | |
| Layer No. | Via | Description | Layer Name | Material Type | Dielectric Constant | Dielectric Thickness | Copper Thickness | Trace Clearance | Trace Width | Current (Amps) | Characteristic Impedance (Zo) | Edge Coupled Differential (Zdiff) | Broadside Coupled Differential (Zdbs) |
| 1 | 8 | Signal | Top | Conductive | | | 1.4 | 5 | 20 | 1 | 47.9 | 72.19 | |
| | | Prepreg | | Dielectric | 4.3 | 10 | | | | | | | |
| 2 | | Plane | GND | Conductive | | | 1.4 | | | | | | |
| | | Core | | Dielectric | 4.3 | 8 | | | | | | | |
| 3 | | Plane | GND | Conductive | | | 1.4 | | | | | | |

| Stackup Planner PDN Planner CPW Planner | | | | | | | | | | | | | |
|--|-----|-------------|------------|---------------|---------------------|----------------------|------------------|-----------------|-------------|----------------|-------------------------------|-----------------------------------|---------------------------------------|
| 2 Layer 4 Layer 6 Layer 8 Layer 10 Layer 12 Layer 14 Layer 16 Layer 18 Layer 12 Layer addc | | | | | | | | | | | | | |
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| Differential Pairs > 100 ohm Differential | | | | | | | | | | | | | |
| Layer No. | Via | Description | Layer Name | Material Type | Dielectric Constant | Dielectric Thickness | Copper Thickness | Trace Clearance | Trace Width | Current (Amps) | Characteristic Impedance (Zo) | Edge Coupled Differential (Zdiff) | Broadside Coupled Differential (Zdbs) |
| 1 | 8 | Signal | Top | Conductive | | | 1.4 | 5 | 20 | 1 | 70.07 | 100.34 | |
| | | Prepreg | | Dielectric | 4.3 | 10 | | | | | | | |
| 2 | | Signal | GND | Conductive | | | Plane cut out | | | | | | |
| | | Core | | Dielectric | 4.3 | 8 | | | | | | | |
| 3 | | Plane | GND | Conductive | | | 1.4 | | | | | | |

Figure 4: 100Ω impedance when the plane beneath the capacitor is removed (source: iCD Stackup Planner).

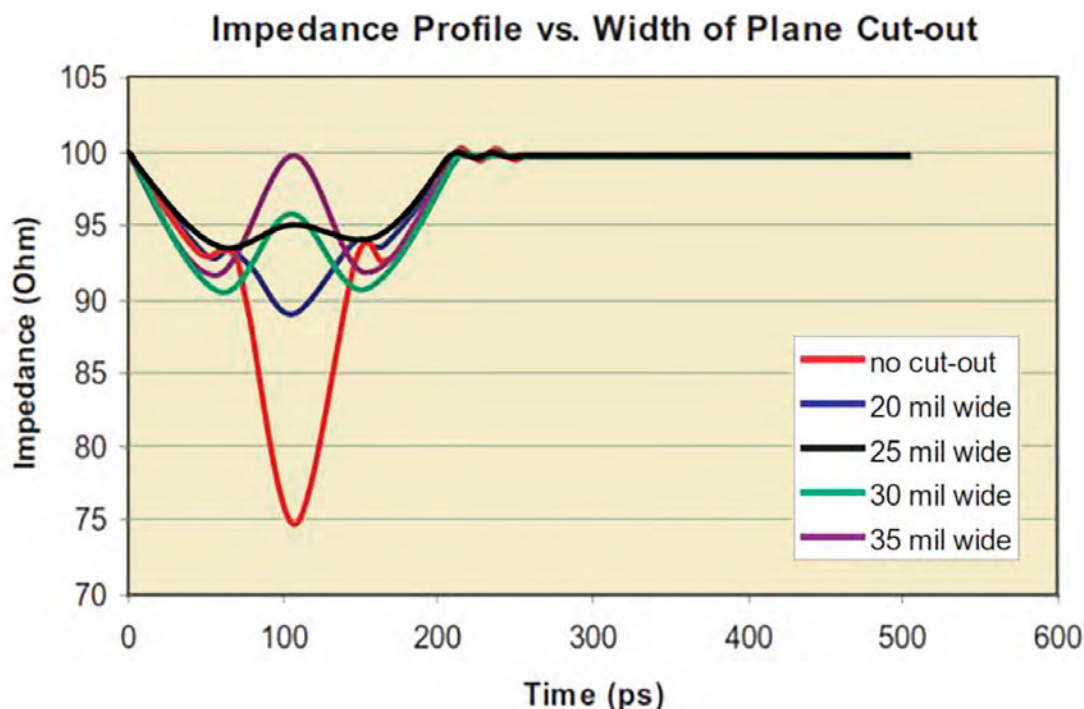


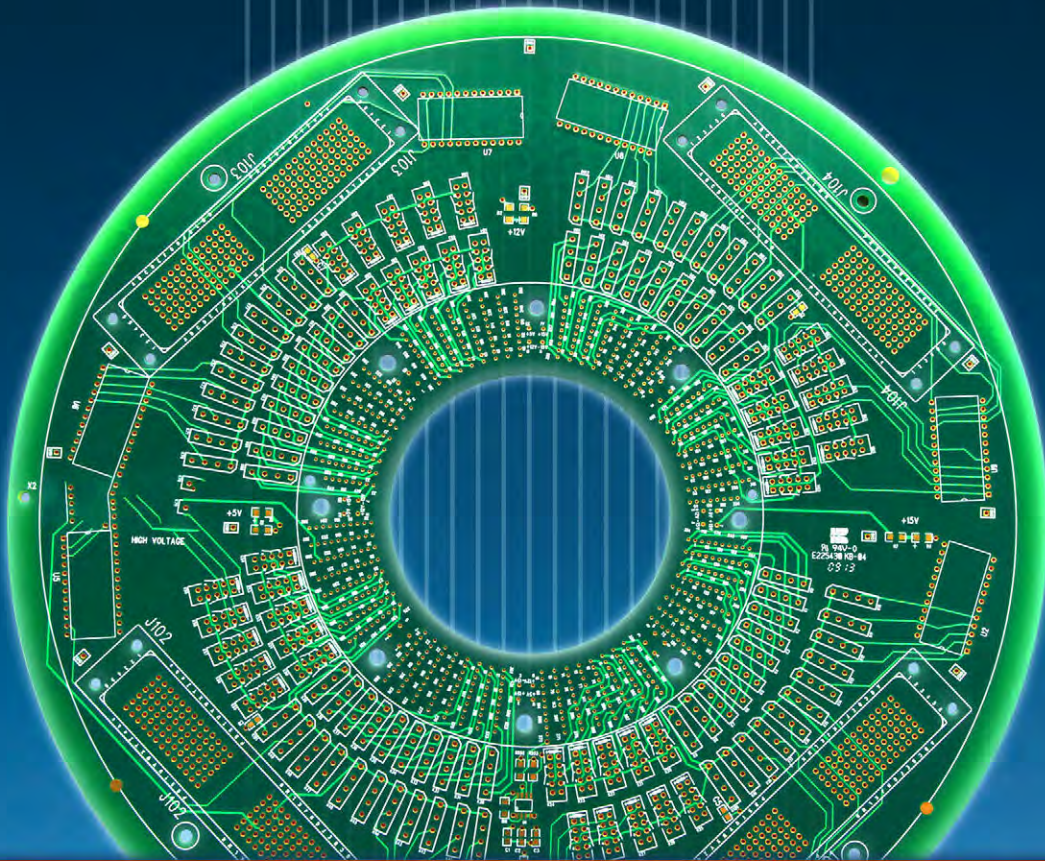
Figure 5: TDR simulation of impedance profile vs plane cut out width (source: Altera).

to estimate the impedance, to the lower plane on layer 3, by swapping the layer 2 plane for a signal layer as depicted. This increases the impedance from 72 to 100Ω.

The four ground vias near the AC coupling capacitors and the two on the connector lands, in Figure 3, are essential to provide a direct current return path to the lower GND plane

and back. Vias correctly placed will serve to minimize crosstalk and contain the common modes that propagate due to signal skew. Common mode conversion near the receiver can have some disastrous multi-aggressor crosstalk peaking implications.

Figure 5 shows a TDR impedance plot from an Ansoft HFSS simulation. The red line is the



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impedance profile of the high-speed differential traces without the plane cut out under the surface mount lands of the AC coupling capacitors. The other lines are the impedance profiles with the cut out set to different widths.

The simulation results show that the width of the plane cut out plays an important role in minimizing the impedance mismatch. The impedance without the plane cut out is below 75Ω at the capacitor lands. However, this needs to be increased to 100Ω to avoid reflections. The minimum impedance mismatch and therefore the optimum structure is achieved when the width of the cut out is 25mils. For most applications, a capacitance value of 100nF with a 0402 package, for the AC coupling capacitor, is adequate.

This is a basic guideline to follow if you do not have access to a simulation tool. If the lower plane is a power plane or if there is no lower plane, a ground fill can be poured in the region underneath the capacitors and stitched with four GND vias close to each capacitor land.

Systems fail for all sorts of reasons, and some of the issues relate to the interaction between reflections across multiple components. Optimization is free, and margin-engineering is a non-recurring expense, and as such is free with regards to manufacturing costs. Once done, the margin is always there and costs nothing to implement.

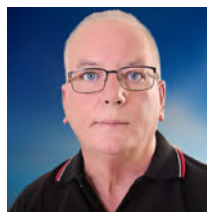
Key Points

- Discontinuities in the physical geometries, along the transmission path, degrade the signal by loss of amplitude, reduction of rise time, and increased jitter.
- A capacitor is typically placed in series with both differential signal traces to remove common mode voltage differences.
- AC coupling is useful because the DC component of a signal acts as a voltage offset, and removing it can increase the resolution of the signal and allows different technologies to communicate.
- The most important parameter of the AC coupling capacitor is the relative geometry with respect to its environment.

- It does not matter where an AC coupling capacitor is placed along the transmission path.
- The capacitor transition is critical: how low the reflectivity is, and whether it is placed near other channel discontinuities.
- AC coupling removes the common mode level and allows the receiver to set its own bias point.
- To eliminate the excess parasitic capacitance, associated with surface mount lands, a portion of the reference plane, that is directly beneath the component, can be removed.
- Ground vias placed near the AC coupling capacitors are essential to provide a direct current return path to the lower GND plane and back.
- The minimum impedance mismatch and therefore the optimum structure is achieved when the width of the cut-out beneath the capacitor is 25 mils.
- For most applications, a capacitance value of 100nF with an 0402 package for the AC coupling capacitor is adequate.

References

1. [DC Coupling with 7 Series FPGAs GTX Transceivers](#), Xilinx.
2. [Optimizing Impedance Discontinuity Caused by SM Pads for High-Speed Channel Designs](#), Altera.
3. [AC and DC Coupling: What's the Difference?](#) Siemens.
4. [High-Speed Digital Design](#), Howard Johnson.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner. The software can be downloaded from www.icd.com.au. To contact Olney, or read past columns, [click here](#).

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The challenges include:

- Handling and protecting thin and small components made from brittle materials (silicon, III-V compounds, etc.)
- Flexible interconnects on a wide range of scales from microns to millimeters
- Reliability with thermal expansion coefficients of different components ranging from a few ppm to hundreds
- Cost-effective process techniques for putting it all together

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FAQ: Encapsulation Resins

Sensible Design

Feature Column by Alistair Little, ELECTROLUBE

A while ago, I took over the reins of this column from my colleague, Phil Kinner, who covered the subject of conformal coatings in his excellent series of columns. Following my own series of columns on encapsulation resins, Jade Bridges has provided some useful hints and tips on thermal management materials and their role in the protection of vulnerable electronic assemblies. We hope these tutorials have given readers a better understanding of how high-performance electro-chemicals, when appropriately selected and correctly applied, can prolong the service life of critical electronic systems exposed to environmental extremes and adverse operating conditions.

I've been invited once more to be a guest writer for this column and I'm very happy to continue with my specialty subject: resins. For this month's column, I have selected five questions that are frequently asked by our customers. I believe they will help set the scene for an informative sequel to my last series.

Q Extreme environmental conditions are often encountered in the

bid to offer protection for PCBs. How do resins offer this protection?

A Several different factors influence the way resins provide protection. The act of encapsulating a component or PCB means that it is surrounded by a layer of resin, which, since it is normally done in a single operation, completely seals a component or an entire PCB from the environment in which it operates. A two-part resin, when mixed, starts a chemical reaction which results in the resin becoming fully polymerised to provide a homogenous layer. The polymerisation reaction creates a three-dimensional structure which provides a barrier against chemical attack and high humidity, for example, and even physical shocks and the destructive effects of thermal cycling.

Q Under less extreme conditions, is a resin still the best option or should a coating be considered as an alternative? What pointers will assist a design engineer to make the choice between these two approaches?

A This is an interesting point, as the protection provided by a coating offers many advantages over the application of a resin. However, as always, the choice will depend upon what level of protection the PCB designer requires. As a rule of thumb, though, to ensure the highest levels of protection, resins are, overall, superior to coatings.

A note of caution here: if weight or volume is a paramount consideration, then a coating is preferred, as this is likely to provide adequate protection while ensuring minimal weight/volume increase. On the other hand, if you need to protect your intellectual property and preclude the



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underlying circuit from being copied, then a resin will not only provide excellent protection due to its toughness, chemical resistance and adhesion to the substrate and components, but with pigmented resins, its opacity will ensure that the circuit detail is visually obscured. It is well to remember that some filled resins are also X-ray opaque!

Q Why are silicone resins appropriate choices for high temperature applications that also demand protection against harsh environmental conditions?

A Silicone resins have the broadest continuous operating temperature range of any of the resin chemistries that we currently offer, so they are a natural choice for both high and low temperature applications. They maintain their flexibility over this temperature range with very little signs of degradation over time. Due to their high flexibility, they place very low stresses on delicate components, particularly those with weak and fragile connecting legs.

There is, however, a downside to silicones, particularly the effectiveness of their adhesion to certain substrates. Moreover, their chemical resistance is not as good as that provided by an epoxy resin. Another category of resins—polyurethanes—would be the better choice for applications operating in the -30 to +120°C region as these offer similar levels of flexibility and better adhesion to many substrates, and all for a lower price.

Q How do resins work to reduce damage to PCBs from vibration?

A Due to the crosslinking that takes place during the curing of the resin, a three-dimensional structure is created which can absorb stresses and strains and help to distribute the forces involved over a larger volume. By doing so, the magnitude of the forces acting upon a component is considerably reduced compared to that of a non-potted component. The same reasoning applies to both physical and thermal shocks. In these cases, the thicker the resin

layer applied, the greater the level of protection that is provided.

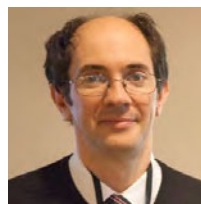
Q Optically clear resins are ideal for LED applications (for example protection of the LED itself), so why is UV stability so important for these resins?

A For LED lighting units, particularly those installed outdoors and in all weather, UV radiation is a fact of life, and the single greatest source is the sun. Most of resins have an aromatic backbone (they contain benzene rings), which will turn yellow when exposed to UV light. They will then start to break down over time as the processes that cause yellowing also result in the formation of free radicals, which leads to the breaking of chemical bonds within the structure.

Resins with an aliphatic backbone do not contain aromatic (benzene) rings, and are less likely to turn yellow and subsequently deteriorate. Free radicals are still formed within aliphatic resins, but at a much lower concentration and they do not have as many sites to attack compared to aromatic resins.

Of course, while being the main source of UV light on earth, the sun is not alone in emitting this potentially damaging radiation. Artificial light sources (tungsten, fluorescent, metal halide, for example) all emit certain levels of UV light, which can attack the resin, not to mention the LEDs themselves, which also generate some UV radiation.

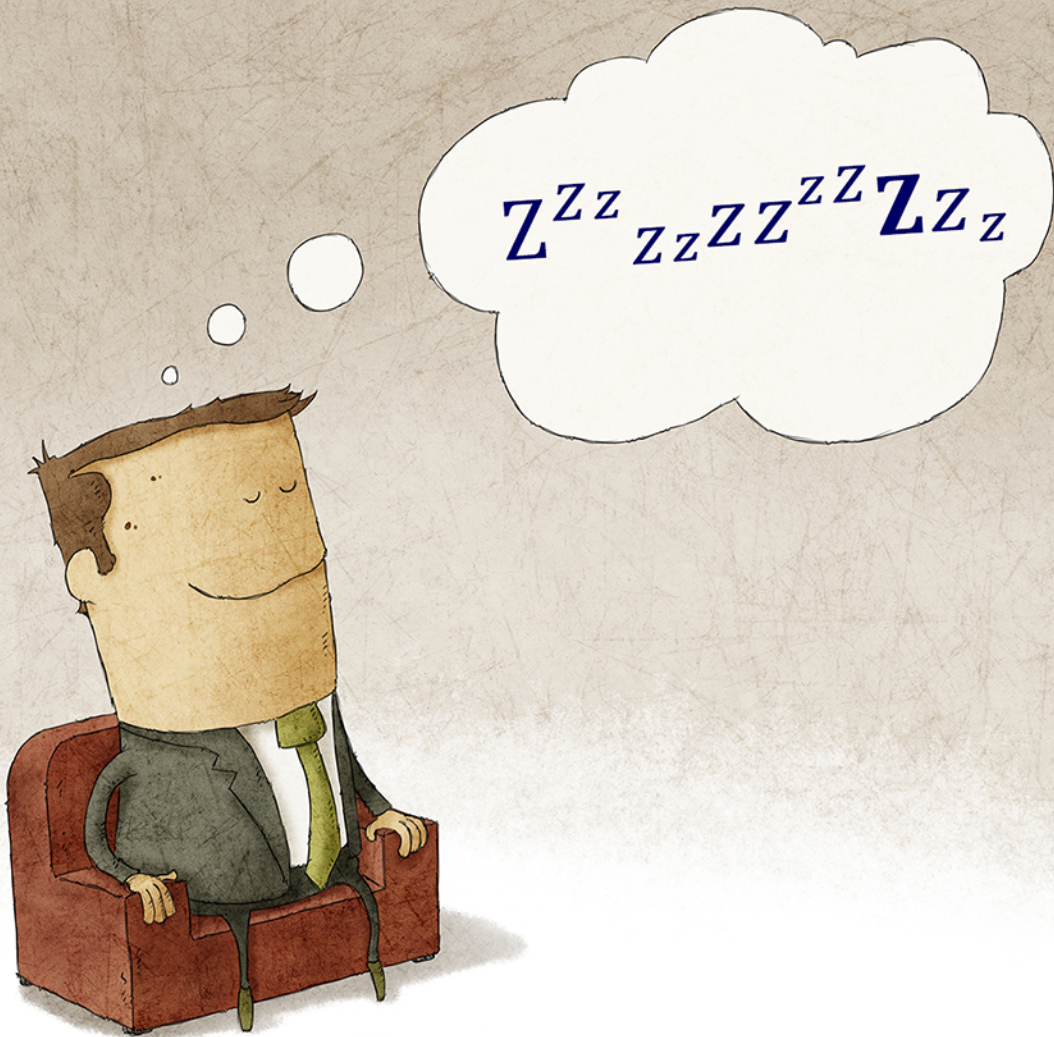
I hope this has been a useful overview that has provided further insight into the effectiveness of resin chemistries. Feel free to get in touch with any of your own queries. Until next time, folks. **DESIGN007**



Alistair Little is global business technical director of Electrolube's Resins Division.

Download Electrolube's free e-book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments*, [here](#).

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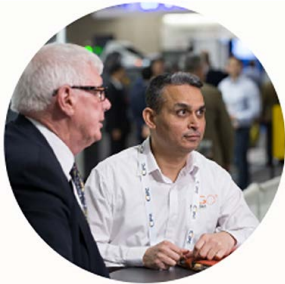
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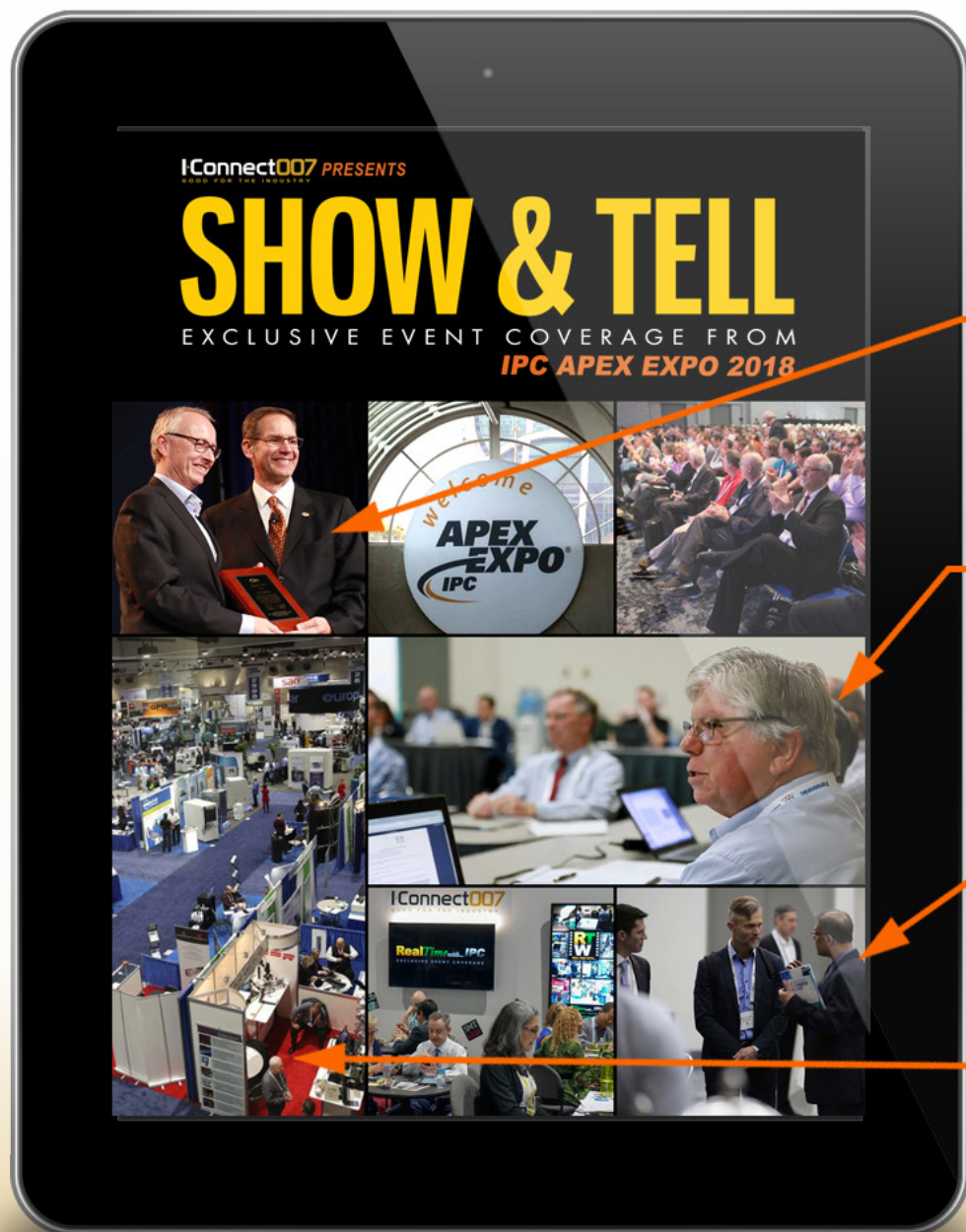


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MilAero Highlights

Beyond Design: Signal Flight Time Variance in Multilayer PCBs ►

A transmission line does not carry the digital signal itself but rather guides electromagnetic energy from one point to another. Signals travel at the same speed, given the same medium. However, the microstrip (outer layer) traces are embedded in a mélange of dielectric material, solder mask, and air.

Merlin Flex Achieves AS9100 Rev D ►

Merlin Flex Ltd, Hartlepool UK, has successfully made the transition from AS9100 Rev C to the latest Rev D. In January 2018, Merlin Flex also maintained their SC21 Bronze award for the 6th year running and is working with Thales UK, the companies SC21 sponsor, in achieving Silver by June 2018.

Improving Military Communications with Digital Phased-Arrays at Millimeter Wave ►

There is increasing interest in making broader use of the millimeter wave frequency band for communications on small mobile platforms where narrow antenna beams from small radiating apertures provide enhanced communication security.

Pioneer Circuits' Solutions Used in NASA's PUFFER Collapsible Bot ►

The PUFFER collapsible micro-rover is a part of NASA's "Game Changing Development Program." It is a compact rover that rides on board with future space vehicles to land on space bodies such as planets and asteroids for photographs and microanalysis.

Flights Show Promising Technologies from Industry and Academic Partnerships ►

The technologies ranged from proposed new space suits to cryogenic propellant research,

with implications for future NASA space missions as well as other research efforts.

Army-led Effort Demos New Atomic Effect for Potential Isotopic Battery ►

A multinational research team, led by Army scientists, successfully induced a controlled release of stored isotopic energy using a physical effect involving atomic electrons. The process was proposed more than 40 years ago but never before demonstrated experimentally.

FTG Releases Full Year and Q4 2017 Financial Results ►

"2017 was a year of transitioning work from the acquired facilities in 2016 to FTG facilities. There were many challenges in the transitions and it took longer than expected but by year end the transitions were complete," stated FTG President and CEO Brad Bourne.

Designing Electronics for Harsh Conditions ►

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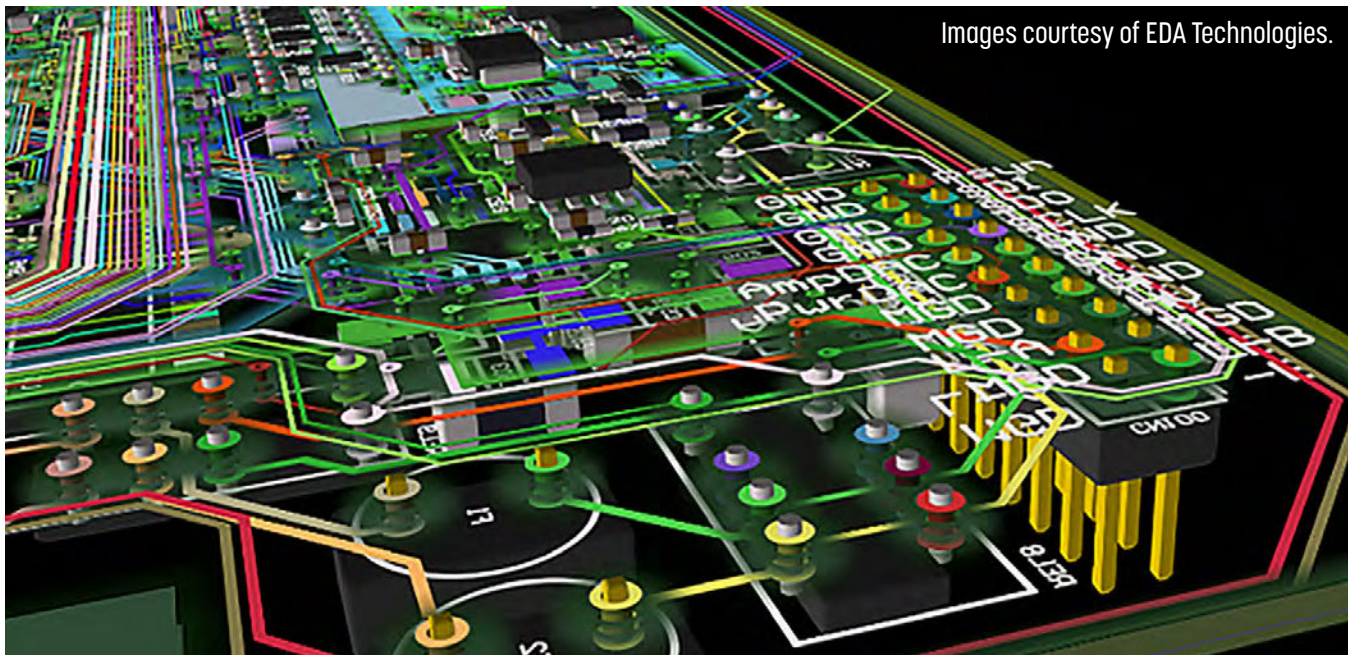
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Images courtesy of EDA Technologies.

South African Electronics Industry Going Strong

by **Barry Matties**
I-CONNECT007

EDA Technologies is a South African company that offers PCB design engineering services, mainly for the domestic electronics market, which makes up a surprising 12.5% of South Africa's GDP. I recently spoke to founder Nechan Naicker about the benefits of outsourcing to South Africa, the market segments they service there, and any advice he had to offer from his 20+ years in the industry.

Barry Matties: First, tell our readers a little bit about your company and what you do?

Nechan Naicker: EDA Technologies is a concept-to-complete electronics solutions company founded over 20 years ago. We've always been involved with PC boards. Back in the day we sold and supported P-CAD, one of the earliest PCB design tools working on DOS, developed by IBM for their own use and later sold off. PCAD changed owners numerous times and

evolved until what we have today in Altium Designer. Over the 20 years of selling and supporting PCB CAD tools, we've obviously done a lot of training.

Being at the bottom tip of Africa, people always imagine that we have lions running around in the streets. They do sometimes, but thankfully not where I live. What's interesting is that most of the people that I speak to have no idea how advanced South Africa's electronics industry is. To give you an idea, a large part of SAAB's electronics engineering is done in South Africa, employing a few hundred engineers. We have many hundreds of engineering contacts in our database, so I would say that South Africa has a thriving and advanced electronics industry.

Matties: Expand a little on EDA Technologies and the services you offer.

Naicker: Originally, we started as a PCB design house, but then we also started to sell and support PCB CAD tools. Today we offer turnkey



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Matties: And you're selling the tools as well?

Naicker: Yes, so we have been a reseller for Altium in South Africa for many years. Altium is the most widely used PCB tool in South Africa. Since we have also used Altium Designer to design exceptionally complex designs, our understanding of the tool is of the highest level so that we can quickly assist our customers with support.



Nechan Naicker

Matties: My understanding is that the Chinese bring a lot of investment and infrastructure into this region as well, such as highways. Is that the case?

Naicker: Yes. Africa is rich in minerals, so copper is a big commodity along with other sought-after minerals. The Chinese investors have purchased entire mineral mines in parts of Africa, like Botswana. In exchange, they may build roads and put up some infrastructure.

Matties: You've been doing design for many years. What sort of design changes have you seen over the years that surprised you?

Naicker: EDA has been designing and manufacturing multilayer PCBs of 12 layers and above for over 15 years now, so this is nothing new. I would say that the technology that intrigued me most recently was the need for embedded copper coin technology. Due to high power demands in electronic systems like RF designs, there's a big need for embedded copper in the PCB to handle the heat distribution and large

currents. So, manufacturers mill out a piece of the PCB, insert precisely crafted copper in the cavity, plate over it, and the result is one of the best thermal conductivity solution available on PCBs.

Matties: How big is the electronics market in SA?

Naicker: The market is large. As I mentioned, electronics makes up 12.5% of our GDP. For a country that's rich in minerals, agriculture and tourism, 12.5% is a fair chunk.

Matties: Is it domestic or mostly international work that is coming your way?

Naicker: Most of our work is from our domestic market. South Africa has a large electronics industry with lots of electronics graduates every year, so we've got a rich pool of skills. We have several

multinational companies in South Africa like BAE Systems and Siemens, so many locally designed products are then shipped overseas to Europe and USA.

Matties: What's the advantage of doing business in South Africa?

Naicker: The big advantage is that we've got a very skilled engineering base who are multi-talented. In some countries engineers are assigned just a piece of a project. But in South Africa, engineers can do the entire project, from the power electronics to the high speed, to the RF and so on. So that's one advantage of using engineering services from South Africa. The other benefit is that our labor cost is lower than Europe or the States.

Matties: By what degree, do you think?

Naicker: It depends really, but in some cases, we can be around 30% cheaper.

Matties: That's in line with China.

Naicker: Yes, we are competitive. Many companies such as iPulse and Sierra Monitor are based in the USA, but their development work is done in South Africa. In the past, I've done work for companies like Flextronics, even National Semiconductor, mainly because of our in-house experience and the lower cost of development.

Matties: What do you look for in a designer when you're hiring for your facility?

Naicker: Skills can be taught, but attitude is harder to teach, so we always look for the right attitude. Also, a person must have a passion for what he's doing, and he must have a level of competence, obviously.

Matties: Those are hard qualities to understand until after you've worked for somebody for a while. How does that process work, then?

Naicker: South Africa is very strict with labor laws, so you can't just hire and fire. We go through an interview process which could be two or three sessions and do as much as we can in terms of doing some background checks on the person, an aptitude test, and that's the best we can really do. But generally, the attitude is good.

Matties: Is there a lot of interest in the young people becoming circuit board designers in South Africa? I know in other regions it's not viewed as a glamorous career and I'm wondering how it's perceived there.

Naicker: PCB design is not pursued as a glamorous career, but we have many EE graduates each year, and obviously PCB design is fundamental to what they do. Most of the universities in South Africa use Altium Designer, so the nice thing is that when they come out of university they are almost ready to be placed into companies. Generally, we turn out many thousands of engineers every year that are very capable. To give you an example, we are currently doing some interesting projects, such as designing a head for a drone, to detect gas leaks in underground mines. In the past canaries were used for this mission. We're doing another project involving a power management system for autonomous trucks in the mines. So there's quite many interesting projects that we're doing for customers.

Matties: How many local circuit board fabricators are in your region?

Naicker: I would say less than 10.

Matties: So a small pool to choose from for some quick turn stuff, but it's there for you guys?





so that creates some challenges for manufacturing. But more and more PCB designs are being forced to go that way because of the dense topology on the boards.

Matties: You've been doing this for many years. What advice would you give a circuit board fabricator from a designer's point of view?

Naicker: Yes, we've got some local companies that can manufacture around 12-layer PCBs, but not necessarily in high volume. Usually any product destined for high volume or which utilizes advanced technologies such as buried capacitance or laser drilling would normally be sent offshore.

Matties: How much of the business that comes through there winds up going offshore? Do they use your service or do they have their own channels to get it accomplished?

Naicker: There's always the fear factor of dealing directly in China. However, since EDA has been doing this for over 20 years, we have established strong relationships with approved suppliers, and we've also built a level of trust and confidence with our customers. EDA manages the full design and manufacturing cycle for clients, so that they can focus on selling their products.

Matties: Are you seeing a demand increase for HDI boards?

Naicker: I would say, yes. The fastest-growing segments in our local PCB market are flex-rigid and HDI boards.

Matties: In terms of HDI, what's the greatest challenge from a design point of view that you see?

Naicker: The greatest challenge I would say is really the drill stacks. For very complex PCBs requiring dense routing of the traces, we often have stacked vias, one on top of the other,

Naicker: For a fabricator, share your knowledge, share information. The biggest pitfall with many designers is that they go full steam ahead with a design, but then sadly due to poor design and material choices, the board may not be manufacturable. It is best if manufacturers share more of their knowledge up front with their customers.

Matties: When we talk about not being manufacturable, there are simulation tools and a lot of other resources like DFM tools. Why do we get to the point where it's at the fabricator before we've realized it's not manufacturable?

Naicker: I think a lot of it has got to do with ignorance, unfortunately, because we should know what the capability of a factory or a fabricator is before we go down the path. The designer should work with reputable suppliers or suppliers they're familiar with, find out the capabilities and the roadmap, and design accordingly—not wait until the end.

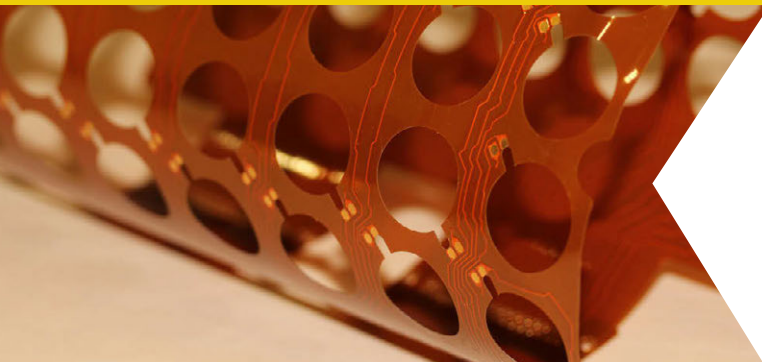
Matties: What sort of feedback is the most valuable that you could receive from a fabricator, post-production?

Naicker: If they could come back and tell us, "We managed to do your board, but in the future if you just increase the annular ring by 'X' amount, your yield will increase." Then we wouldn't be repeating poor choices and we would in effect lower the cost of manufacture.

Matties: Have you ever known a fabricator to just provide you that information, or is this something that unless you ask for it they don't share it?

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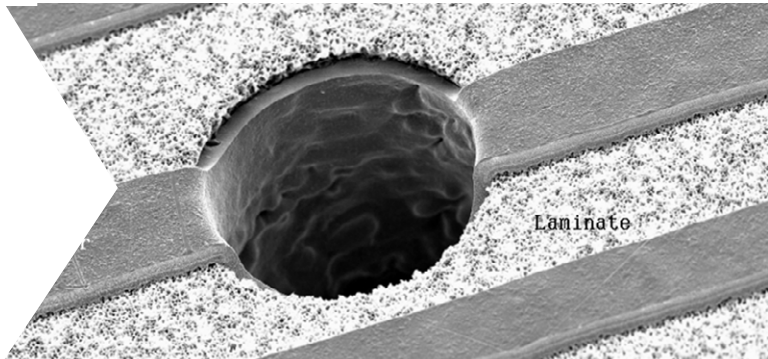


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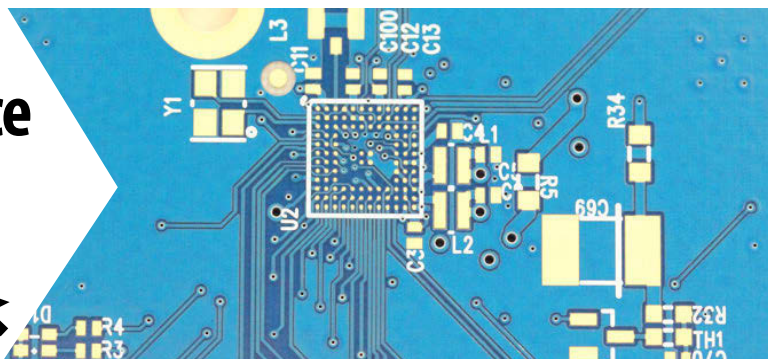
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Naicker: We've had a good relationship with a very reputable global PCB supplier called NCAB Group, with HQ in Sweden and offices throughout the world. They are open to sharing their knowledge and often give us feedback for improvement.

Matties: It's for everybody's benefit to do that—theirs, yours, and ultimately, the end customer.

Naicker: Of course. Because every company needs to be competitive on the world scene, getting feedback like that can improve the yield, also any yield loss is not factored into the final product cost. Everyone wins.

Matties: I would think that having a fabricator who's proactive in providing feedback, that a purchaser of PCBs would even be willing to pay a little extra because of the confidence in knowing that they're going to have a quality product.

Naicker: Exactly. We've made, on some products, many hundreds of thousands of boards over the last years with not one single failure, so it is possible. Price is what you pay, value is what you get. The key factor with modern PCBs is reliability and repeatability. If you really want that, you may need to pay a small surcharge, but it's worth it in the end. We say, "good quality is expensive, poor quality is even more expensive."

Matties: What advice would you give a young designer just entering in to the design community?

Naicker: One of the biggest pieces of advice I would give them is first build up your knowl-

edge base on good design practices. I attended Lee Ritchey's high-speed course about four or five years ago in Bitburg, Germany, and having done boards for over 25 years, I really could kick myself for not doing this course earlier. Ever since then, we applied many of the principles we learnt, which will never change because it's a science, and we've had tremendous success with very complex boards working first time

and passing EMC first time. So that investment in your knowledge and design practices is invaluable.

Matties: It certainly sounds like great advice. Is there anything that we haven't talked about that you would like to share with the industry?

Naicker: Yeah, there's one trend that's happening that some people feel very maybe sour about, and that's the globaliza-

tion trend. We saw yesterday in Lee Ritchey's presentation that from 1,200 fabricators in the States over 30 years ago, there are only 200 now. And it's a trend that's happening worldwide, but not just in PCB bareboard manufacture, but also in EMS services. My advice is for companies to focus on their core competencies, and outsource the non-core functions elsewhere to remain competitive. Instead of being sour about it, let's outsource what we need to outsource so that we can continue to make great products for new markets that were not there yesterday.

Matties: Great advice. Thank you so much for spending time with me today.

Naicker: It's a pleasure. DESIGN007

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1 Advanced Circuits Upgrades Free PCB Design Software ►

Advanced Circuits has released version 4.0 of PCB Artist. The free design software offers many features and functionality found in paid PCB design packages without the price tag. PCB Artist includes advanced layout capabilities, a library of over 500,000 components, and free technical support.

3 Altium Delivers Record Revenue Growth of 30% in First Half of Fiscal 2018 ►

Continuing its growing momentum, Altium achieved record revenue growth of 30% for the first half at US\$63.2 million and expanded profit margins to record levels with EBITDA over 30% and a 51% increase in net profit after tax to US\$14.9 million.

2 RTW IPC APEX EXPO: Valor Tool Benefits from Merging Mentor, Siemens Technologies ►

Oren Manor, director of business development, discusses the convergence of the electrical and mechanical disciplines made possible through Mentor's merger with Siemens. Manor also explains how Mentor's Valor platform now utilizes Siemens' "digital twin" concept.



4 Power Integrity by Example eBook Available for Download ►

The Printed Circuit Designer's Guide to... Power Integrity by Example provides a thorough investigation of power distribution network performance. Mentor's Fadi Deek addresses problematic issues within electronic transmissions, and presents a variety of simulations and analyses in every chapter. Readers will gain a better understanding of cause-effect relationships between varying factors and how to consider these when making design decisions.

5 Mentor Launches HyperLynx Solution with Automated and Intelligent Channel Extraction for SERDES Interfaces ▶

Mentor's new HyperLynx PCB simulation technology for high-performance designs now providing the industry's first end-to-end fully automated SERDES channel validation solution. This is the industry's first fully automatic validation tool for PCB SERDES interfaces.

6 IoT: Let's Put the "A" Back into EDA ▶

If I say IoT, most people today will immediately conjure up some notion in their mind. This is especially true in the engineering community, where many of us are hanging the future of our careers on the Utopian vision of a clean, beautiful environment with hidden networks and sensors everywhere. Whatever your viewpoint is, one thing is abundantly clear: there are going to be lots and lots and lots of PCBs made.



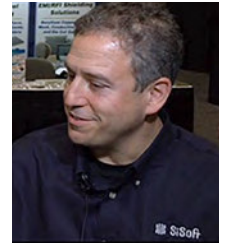
7 DfR Solutions Wins IPC APEX EXPO Innovation Award ▶

DfR Solutions' newest version of its Sherlock Automated Design Analysis Software version 5.4 with temperature-based FEA has been awarded an IPC APEX EXPO Innovation Award. The award was presented to DfR Solutions at IPC APEX EXPO during John Mitchell's keynote speech.



8 Barry Katz Discusses SiSoft's DesignCon Papers and Plans for 2018 ▶

SiSoft President and CTO Barry Katz sat down with Editor Andy Shaughnessy to share his thoughts on the company's papers presented during DesignCon 2018, as well as SiSoft's latest products and plans for 2018.



9 Still Using 1980s Formats for Design Data Handoff? ▶

The IPC-2581 format was created in the early 2000s with the merger of two competing formats: ODB++ and GENCAM. The new format, the brainchild of the late Dieter Bergman, languished with no adoption until 2011, when a small group of companies created the IPC-2581 Consortium with the goal of getting this open, neutral and intelligent format adopted.



10 RTW IPC APEX EXPO: Polar Instruments Discusses New Engineer, SpeedStack Upgrades ▶

During IPC APEX EXPO 2018, Polar Instruments' Lupita Maurer and Geoffrey

Hazelett sat down with Editor Andy Shaughnessy to discuss upgrades to their SpeedStack tool and Lupita's new position with the company.



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- Excellent oral and written communication skills
- Decision making skills and the ability to multitask

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- A minimum of seven years related experience or training in the manufacturing sector or the equivalent combination of formal education and experience
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- Provide feedback to management regarding performance
- Create and conduct customer technical presentations
- Develop technical strategy for customers
- Possess the ability to calm difficult situations with customers, initiate a step by step plan, and involve other technical help quickly to find resolution

Hiring Profile

- Bachelor's Degree or 5–7 years' job-related experience
- Strong understanding of chemistry and chemical interaction within PCB manufacturing
- Excellent written and oral communication skills
- Strong track record of navigating technically through complex organizations
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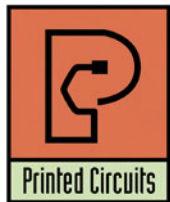
- BSc in electronics engineering
- At least 5 years of R&D experience in complex board design, mainly FPGA (communication interfaces, DDR controller, algorithm implementation)
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- Complete other sales and/or marketing tasks as required

Education and Experience:

- At least 2 years of previous customer service center experience
- Ability to work with Microsoft (MS) Office, with focus on demonstrated working knowledge of MS Excel and Word
- Ability to work well in time-sensitive situations where customer satisfaction is the goal
- Ability to apply creative problem-solving techniques to situations using sound business judgment
- Excellent verbal and written communication skills
- Ability to multi-task in an effective, timely and professional manner
- Proven ability to apply attention to detail, role-related accuracy and task follow-through
- Willingness to learn new software products such as ACT!
- Bachelor's degree a plus

[apply now](#)



The Future in Focus

Field Application Engineer

Saki America Inc., headquartered in Fremont, CA, a leader in automated inspection equipment, seeks two full-time Field Application Engineers (FAE), one in the Fremont headquarters and the other for the Eastern and Southern United States.

The FAE will support the VP of Sales and Service for North America in equipment installation, training, maintenance, and other services at field locations. The FAE will provide technical/customer support and maintain positive relationships with existing and future customers.

Strong analytic abilities and problem-solving skills are a must in order to understand customer applications and troubleshoot issues. The FAE will perform demos and presentations for customers and agents as well as assisting in trade show activities. Candidate must have a minimum of a two-year technical degree, experience in AOI, SPI, and X-ray inspection, and strong verbal and written communication skills. The position requires the ability to travel about three weeks per month. Must be a US citizen and be able to lift up to 40 lbs.

[apply now](#)

Career Opportunities



Business Development Representative at Altium

New Logo Business Development representatives are highly motivated and hardworking with an upbeat can-do attitude. They work with our New Logo Sales Team to displace our competition in accounts by offering Altium's unified PCB development tools within a defined region.

The New Logo Developer's (NLD) main responsibilities will be qualifying leads and prospecting into competitive lists, searching the web, and utilizing internal sales tools (Inside View, LinkedIn, Marketo, Salesforce) to uncover and work with opportunities for the New Logo Closer to close. They are expected to meet or exceed monthly, quarterly & annual quota.

Responsibilities:

- Develop lead opportunities by collecting information that includes business pains/needs, timelines, authority and project teams, budget, competitive information, etc.
- Aggressively drive daily prospecting calls to build pipeline of prospective clients and occasionally closing smaller deals
- Develop relationships with key partners in their territory to identify new business opportunities
- Plan and prioritize personal sales activities in conjunction with the New Logo Closer, with the goal of achieving sales targets
- Work alongside inside sales teams on specialized projects such as call-out campaigns, promo drives and webinar fulfillment
- Once trained, maintain an in-depth knowledge of Altium products and technologies, competitive products, and industry trends.

[apply now](#)



Field Service Technician

Chemcut, a leading manufacturer of wet-processing equipment for the manufacture of printed circuit boards for more than 60 years, is seeking a high-quality field service technician. This position will require extensive travel, including overseas.

Job responsibilities include:

- Installing and testing Chemcut equipment at the customer's location
- Training customers for proper operation and maintenance
- Providing technical support for problems by diagnosing and repairing mechanical and electrical malfunctions
- Filling out and submitting service call paperwork completely, accurately and in a timely fashion
- Preparing quotes to modify, rebuild, and/or repair Chemcut equipment

Requirements:

- Associates degree or trade school degree, or four years equivalent HVAC/industrial equipment technical experience
- Strong mechanical aptitude and electrical knowledge, along with the ability to troubleshoot PLC control
- Experience with single and three-phase power, low-voltage control circuits and knowledge of AC and DC drives are desirable extra skills

To apply for this position, please apply to Mike Burke, or call 814-272-2800.

[apply now](#)

Career Opportunities



Electronics Team Leader

Orbotech is seeking an Electronics Team Leader to join our electronics team, which develops multi-disciplinary systems, including vision/laser, image processing, and control and automation missions.

What Will Your Job Look Like?

- Lead a team of electronics engineers in a multi-disciplinary environment
- Lead electronic activities from requirement phase to development, integration and transfer, to production
- Be the focal point for other disciplines and projects managers
- Maintain and improve existing electronics platforms

What Do You Need to Succeed?

- BSc/MSc in electronic engineering/ computer science from a well-recognized university
- 5+ years' experience in digital board design, high-speed links, computing embedded systems, and HW/SW integration
- 2–3 years' experience in leading a team of engineers
- Solid skills in complex FPGA design with multi-modules
- Solid skills in high-speed board design, DDR3/4, PCIE, USB, IO, and optic links
- Ability to design and execute end-to-end solutions

Who We Are

Virtually every electronic device in the world is produced using Orbotech systems. For over 30 years, Orbotech has been a market leader in developing cutting-edge inspection, test, repair, and production solutions for the manufacture of the world's most sophisticated consumer and industrial electronics.

apply now



ventec
INTERNATIONAL GROUP
騰輝電子

Ventec Seeking U.S. Product Manager for tec-speed

Want to work for a globally successful and growing company and help drive that success? As a U.S.-based member of the product and sales team, your focus will be on Ventec's signal integrity materials, tec-speed, one of the most comprehensive range of products in high-speed/low-loss PCB material technology for high reliability and high-speed computing and storage applications. Combining your strong technical PCB manufacturing and design knowledge with commercial acumen, you will offer North American customers (OEMs, buyers, designers, reliability engineers and the people that liaise directly with the PCB manufacturers) advice and solutions for optimum performance, quality and cost.

Skills and abilities required:

- Technical background in PCB manufacturing/ design
- Solid understanding of signal integrity solutions
- Direct sales knowledge and skills
- Excellent oral and written communication skills in English
- Experience in making compelling presentations to small and large audiences
- Proven relationship building skills with partners and virtual teams

This is a fantastic opportunity to become part of a leading brand and team, with excellent benefits.

Please forward your resume to jpattie@ventec-usa.com and mention "U.S. Sales Manager—tec-speed" in the subject line.

apply now

Career Opportunities



IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

[apply now](#)



INTERNATIONAL GROUP
騰輝電子

Technical Sales Engineer

Positions available in the Chicago area and California

Do you want to advance your career by joining a globally successful and growing world class CCL manufacturer and help drive that success? As a California-based member of the technical sales team, your focus will be on Ventec's core market segments: mil/aero, automotive and medical, offering a full range of high-reliability materials including polyimide, IMS and thermal management products.

Skills and abilities required:

- Drive & Tenacity!
- 7 to 10 years of experience in the PCB industry in engineering and/or manufacturing
- Detail-oriented approach to tasks
- Ability to manage tasks and set goals independently and as part of a team
- Knowledge of MS office products

Full product training will be provided. This is a fantastic opportunity to become part of a successful brand and a leading team with excellent benefits.

Please forward your resume to:

jpattie@ventec-usa.com and mention "Technical Sales Engineer - California Based or Chicago area" in the subject line.

[apply now](#)

Career Opportunities

Altium®

Application Engineer

The application engineer is the first contact for our customers who have technical questions or issues with our product. We value our customers and wish to provide them with highest quality of technical support.

Key Responsibilities:

- Support customer base through a variety of mediums
- Log, troubleshoot, and provide overall escalation management and technical solutions
- Create various types of topic based content, such as online help, online user guides, video tutorials, knowledge base articles, quick start guides and more
- Distill complex technical information into actionable knowledge that users can understand and apply
- Continually develop and maintain product knowledge

Requirements:

- Understanding of EDA electronic design software, schematic capture and PCB layout software
- Bachelor's degree in electronics engineering or equivalent experience
- Sales engineering and/or support engineering experience
- Circuit simulation and/or signal integrity experience
- Understanding of ECAD/ MCAD market segments
- Understanding of micro controllers, SoC architecture and embedded systems market
- Database experience preferred (i.e., MySQL, PostgreSQL, Microsoft Access, SQL, Server, FileMaker, Oracle, Sybase, dBASE, Clipper, FoxPro) etc.
- Experience with PLM/PDM/MRP/ERP software (Program Lifecycle Management) preferred
- Salesforce experience a plus

Salary based upon experience. Comprehensive benefits package and 401k plan. Openings in USA, UK, and Germany.

For more information, contact Altium.

[apply now](#)



PCB Process Planner

Accurate Circuit Engineering (ACE) is an ISO 9001:2000 certified manufacturer of high-quality PCB prototypes and low-volume production for companies who demand the highest quality in the shortest time possible. ACE is seeking a skilled individual to join our team as a PCB process planner.

Responsibilities will include:

- Planning job travelers based on job release, customer purchasing order, drawings and data files and file upon completion
- Contacting customer for any discrepancies found in data during planning and CAM stage
- Consulting with director of engineering regarding technical difficulties raised by particular jobs
- Informing production manager of special material requirements and quick-turn scheduling
- Generating job material requirement slip and verify with shear clerk materials availability
- Maintaining and updating customer revisions of specifications, drawings, etc.
- Acting as point of contact for customer technical inquiries

Candidate should have knowledge of PCB specifications and fabrication techniques. They should also possess good communication and interpersonal skills for interfacing with customers. Math and technical skills are a must as well as the ability to use office equipment including computers, printers, scanners, etc.

This position requires 3 years of experience in PCB planning and a high school level or higher education.

[apply now](#)

Career Opportunities



PCB Equipment Sales

World-class manufacturer of wet process equipment for the PCB and plating industries, Integrated Process Systems Inc. (IPS) is seeking qualified candidates to fill a position in equipment sales. Potential candidates should have:

- Process engineering knowledge in PCB manufacturing
- Outside sales background
- Residency on the West Coast to manage West Coast sales
- Knowledge of wet process equipment
- Sales experience with capital equipment (preferred)

Compensation will include a base salary plus commission, dependent upon experience.

[more details](#)



PCB Assembly Supervisor— full time Accurate Circuit Engineering— Santa Ana, CA

Position Summary: Responsible for all assembly processes to ensure continued growth as directed by management.

Essential Job Functions:

- Create, implement, and supervise in-house manufacturing facility
- Recruit, hire, train, and supervise assembly floor personnel
- Extensive hands on experience with all aspects of PCB assembly
- Understanding of IPC-A-610 standards
- Research and acquire additional assembly resources
- Gather data on product shortages, lead times, price changes, etc.
- Coordinate the assembly activities with sales to ensure 100% on-time delivery
- Create, implement, and supervise daily quality processes to ensure 100% accuracy
- Document, monitor and review progress of the business unit
- Respond to internal and external customers in a timely manner
- Coordinate walk-through, site audits, etc.

Qualifications:

- Minimum 3 years as operations supervisor of electronics assembly house
- 5+ years' experience in the electronics industry
- Previous experience as a quality or operations supervisor preferred
- Ability to solve practical problems using pre-established guidelines
- Strong facility in Microsoft Office applications
- Excellent verbal and written communication skills
- Ability to work with people of diverse backgrounds
- Highly organized/excellent time management skills
- Ability to perform at the highest level in a fast-paced environment
- Valid California driver's license.

[apply now](#)

**AD SPACE
AVAILABLE
NOW**

For information, please contact:
BARB HOCKADAY
barb@iconnect007.com
+1 916.365.1727 (-7 GMT)

I-Connect007
GOOD FOR THE INDUSTRY

Career Opportunities



FPGA Design Expert

Orbotech is seeking a FPGA Design Expert to join our electronics team, which develops multi-disciplinary systems including vision/laser, image processing and electro-optics.

What Will Your Job Look Like?

- Lead image acquisition and processing activities in the team
- Engage in all aspects of FPGA design activity: requirement phase, coding, synthesizing, verification support and LAB bring up
- Participate in system definitions for current and next generation products
- Collaborate with other teams: SW, algorithm and QA

What Do You Need to Succeed?

- BSc/MSc in Electrical Engineering from a well-recognized university
- Extensive knowledge of VHDL
- 5+ years of FPGA development experience (requirement, architecture, RTL coding, simulation, synthesis, timing analysis, P&R, board level integration and verification)
- Experience in designing and implementing low-latency, high-throughput FPGA designs utilizing PCIe Gen2/3, Gigabit Ethernet, SERDES, DDR3/4
- Experience in complex FPGA such as Altera Stratix-II and Arria 5&10 devices
- Authoring documentation experience such as FPGA specifications and FPGA verification plans

Who We Are

Virtually every electronic device in the world is produced using Orbotech systems. For over 30 years, Orbotech has been a market leader in developing cutting-edge inspection, test, repair, and production solutions for the manufacture of the world's most sophisticated consumer and industrial electronics.

[apply now](#)



Arlon EMD, located in Rancho Cucamonga, California is currently interviewing candidates for **manufacturing** and **management positions**. All interested candidates should contact Arlon's HR department at 909-987-9533 or fax resumes to 866-812-5847.

Arlon is a major manufacturer of specialty high performance laminate and prepreg materials for use in a wide variety of PCB (printed circuit board) applications. Arlon specializes in thermoset resin technology including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, high density interconnect (HDI) and microvia PCBs (i.e., in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001:2008 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customer's requirements.

[more details](#)



Events Calendar

China International PCB and Assembly Show (CPCA) ▶

March 20–22, 2018
Shanghai, China

2018FLEX Japan ▶

April 19–20, 2018
Tokyo, Japan

KPCA Show 2018 ▶

April 24–26, 2018
Kintex, South Korea

Thailand PCB Expo 2018 ▶

May 10–12, 2018
Bangkok, Thailand

Medical Electronics Symposium 2018 ▶

May 16–18, 2018
Dallas, Texas, USA

IMPACT Washington, D.C. 2018 ▶

May 21–23, 2018
Washington, D.C., USA

EIPC's 50th Anniversary Conference ▶

May 31–June 1, 2018
Bonn, Germany

JPCA Show 2018 ▶

June 6–8, 2018
Tokyo, Japan

electronica India productronica India ▶

September 26–28, 2018
Bengaluru, India

electronicAsia 2018 ▶

October 13–16, 2018
Hong Kong

SMTA International ▶

October 16–17, 2018
Rosemont, Illinois, USA

TPCA Show 2018 ▶

October 24–26, 2018
Taipei, Taiwan

Additional Event Calendars



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